SystemC – Modules (01A)

SystemC

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05/14/2012

Please send corrections (or suggestions) to youngwlim@hotmail.com.

This document was produced by using OpenOffice and Octave.

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05/14/2012

Based on the following original work

[1] Aleksandar Milenkovic, 2002
CPE 626 The SystemC Language – VHDL, Verilog Designer's Guide
http://www.ece.uah.edu/~milenka/ce626-02S/lectures/cpe626-SystemC-L2.ppt

[2] Alexander de Graaf, EEMCS/ME/CAS, 2010
SystemC: an overview ET 4351
ens.ewi.tudelft.nl/Education/courses/et4351/SystemC-2010v1.pdf

[3] Joachim Gerlach, 2001
System-on-Chip Design with Systent of Computer Engineering
http://www2.cs.uni-paderborn.de/cs/ag-hardt/Forschung/Data/SystemC-Tutorial.pdf

[4] Martino Ruggiero, 2008
SystemC
polimage.polito.it/~lavagno/codes/SystemC_Lezione.pdf

[5] Deepak Kumar Tal, 1998-2012
SystemC Tutorial
http://www.asic-world.com/systemc/index.html

Module Declaration

Basic building blocks of a SystemC design

Can contain processes (→ functionality)
Can contain sub-modules (→ hierarchy)

```
SC_MODULE( module_name ) {
    // Declaration of module ports
    // Declaration of module signals
    // Declaration of processes
    // Declaration of sub-modules

    SC_CTOR( module_name ) {
        // Module constructor
        // Specification of process type and sensitivity
        // Sub-module instantiation and port mapping
    }

    // Initialization of module signals
};
```

SC_MODULE Macro

A module correspond to a C++ class
class member data ↔ ports
class member functions ↔ processes
class constructor ↔ process generation

```
class module_name : sc_module {
.....
};
```

```
SC_MODULE( module_name ) {
.....
};
```

SC_CTOR Macro

A shorthand of writing the constructor using a macro SC_CTOR.

The constructor does the following:

- Create hierarchy (sub-modules)
- Register functions as processes with the simulation kernel
- Declare sensitivity list for processes
- Accepts one argument only, which is the module name

Modules

- The basic building block
- Encapsulate HW / SW functionality
- Module functionality is achieved
  by means of processes
- Can contain sub-modules
- Can provide private variable/signals.
- Can interface to another modules via
  ports/interfaces/channels

TMP

References

[1] Aleksandar Milenkovic, 2002
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