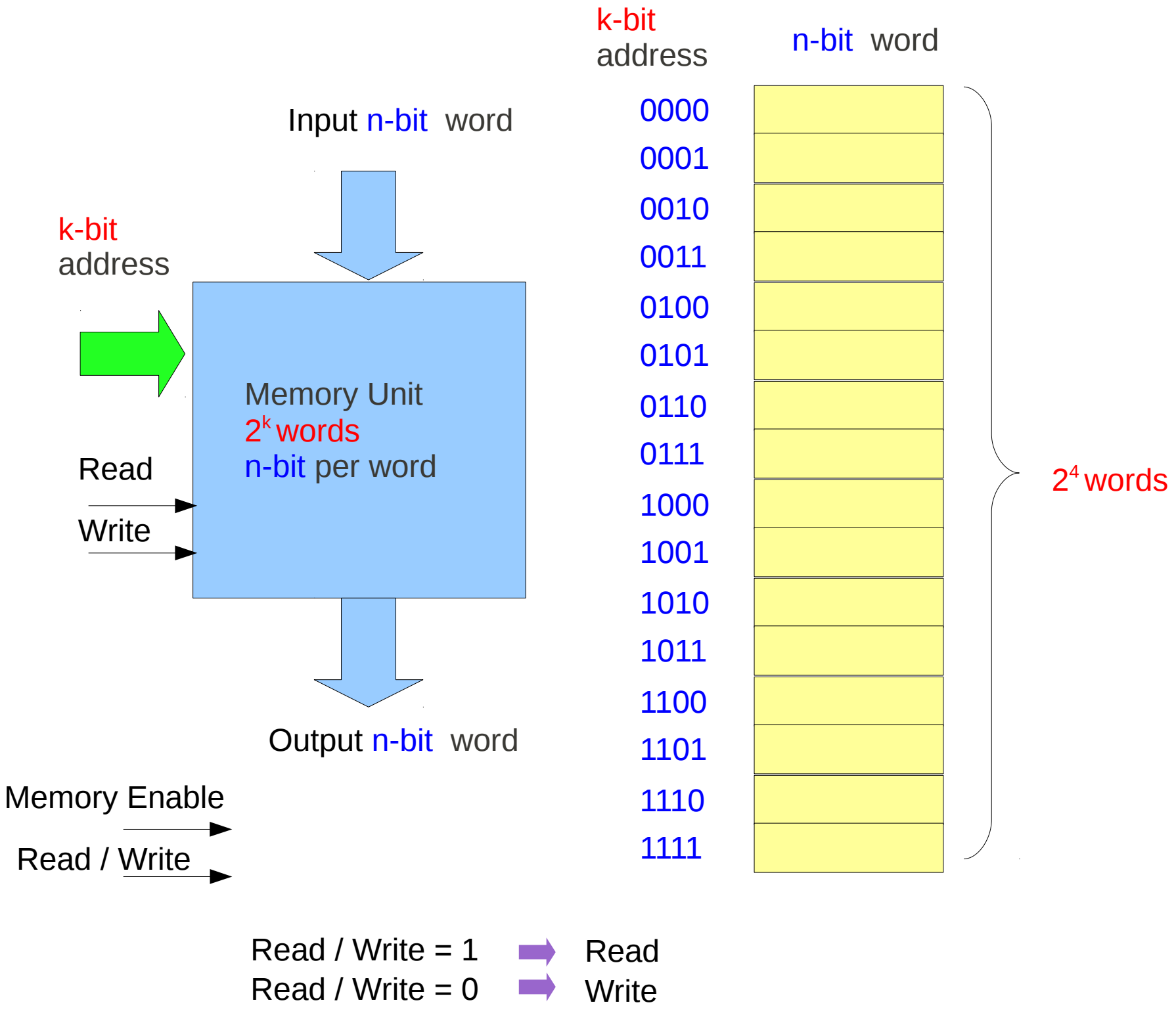
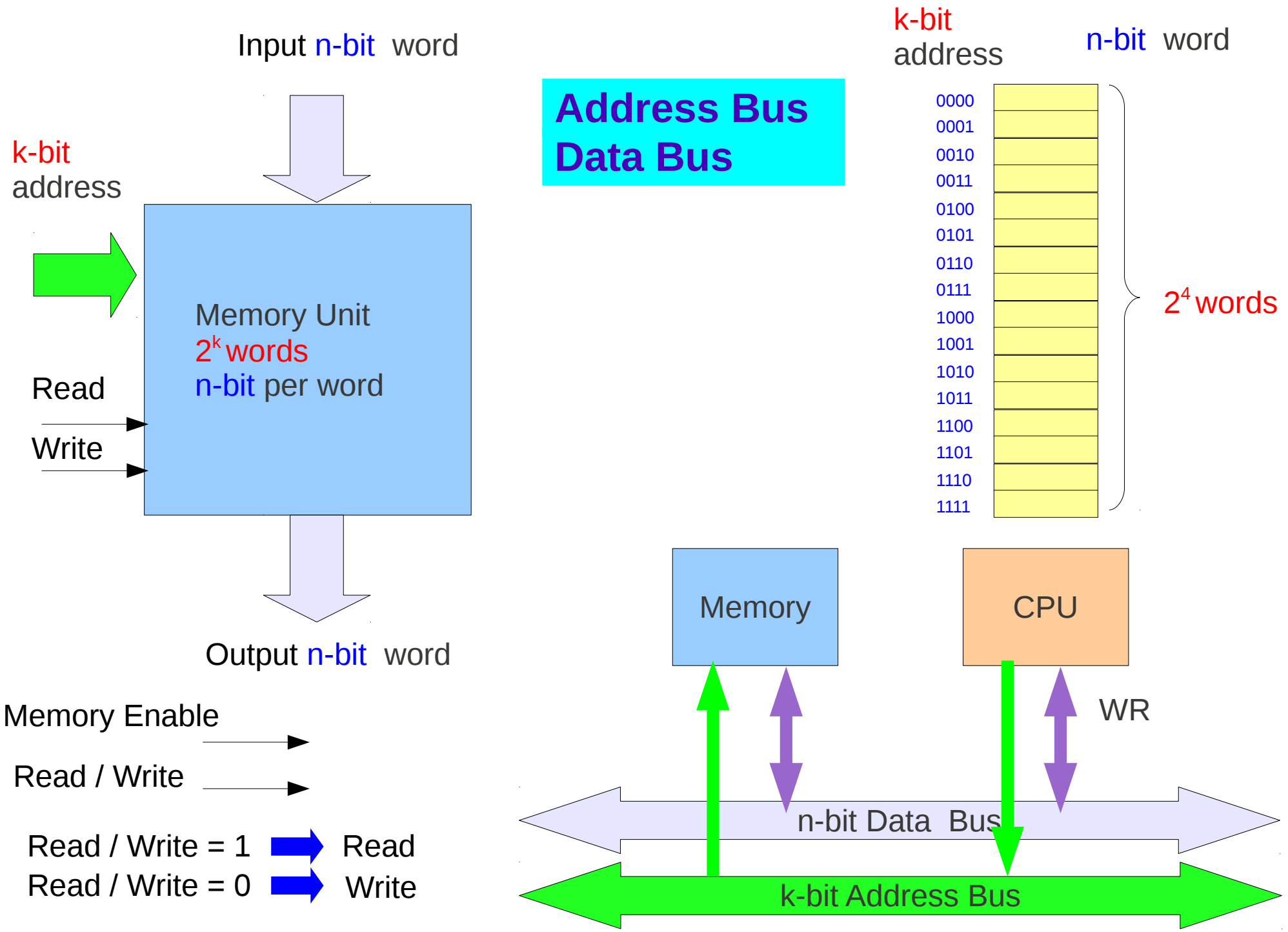
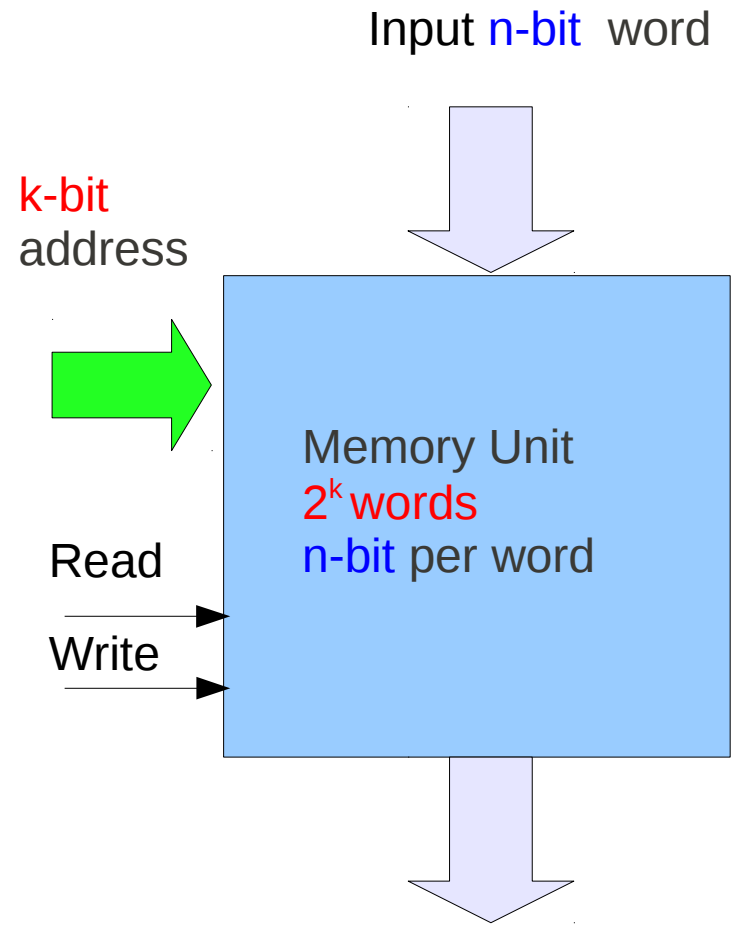
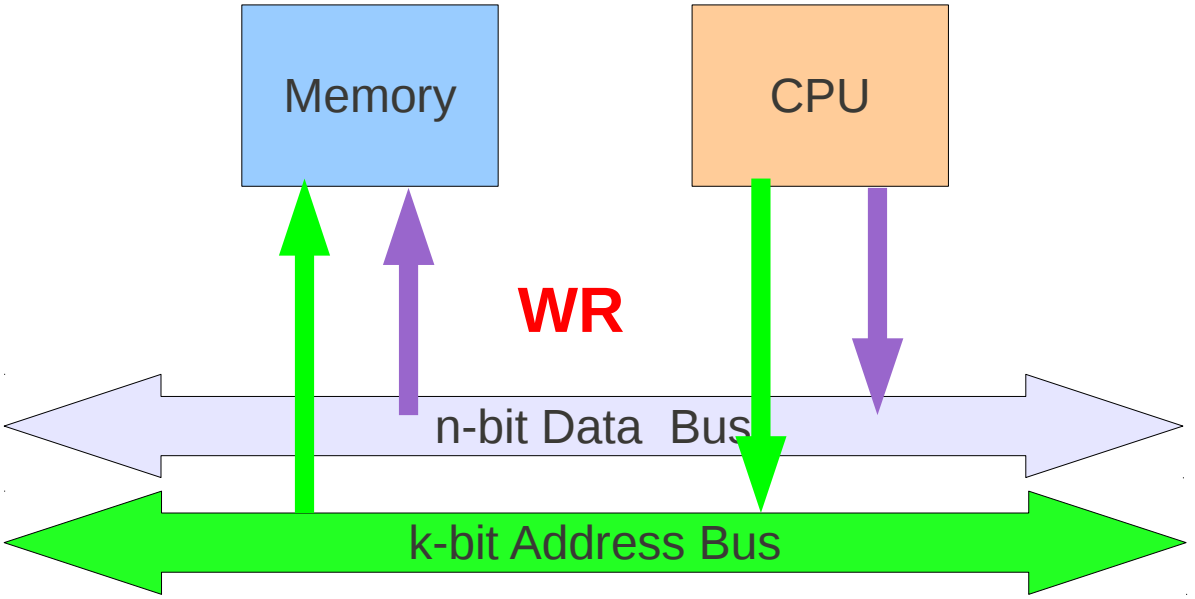
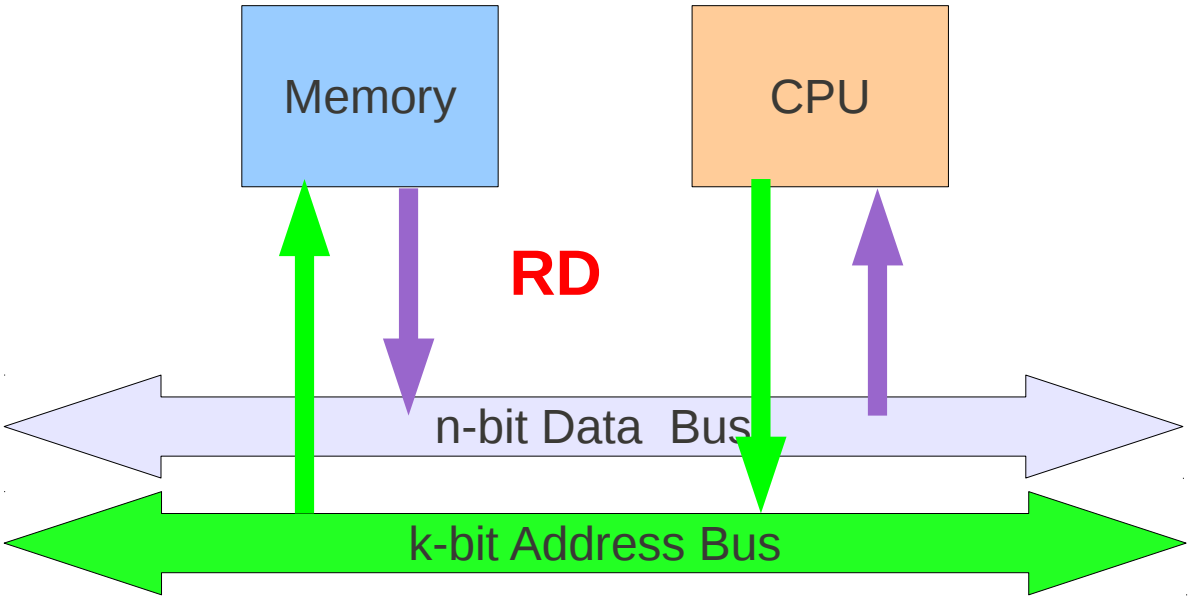

k-bit
address
n-bit word
Input n-bit word
k-bit
address
0000
0001
0010
0011
0100
0101
0110
0111
1000
1001
1010
1011
1100
1101
1110
1111
Memory Unit
2^k words
n-bit per word
Read
Write
2^4 words
Output n-bit word
Memory Enable
Read / Write
Read / Write = 1
Read
Read / Write = 0
Write

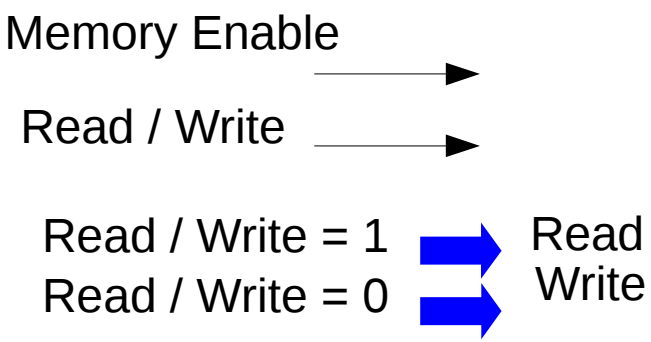

Input n-bit word
k-bit address
Memory Unit
2^k words
n-bit per word
Read
Write
Output n-bit word
Memory Enable
Read / Write
Read / Write = 1
Read
Read / Write = 0
Write
Address Bus
Data Bus
k-bit address
n-bit word
0000
0001
0010
0011
0100
0101
0110
0111
1000
1001
1010
1011
1100
1101
1110
1111
2^4 words
Memory
CPU
WR
n-bit Data Bus
k-bit Address Bus

WR & RD Operations

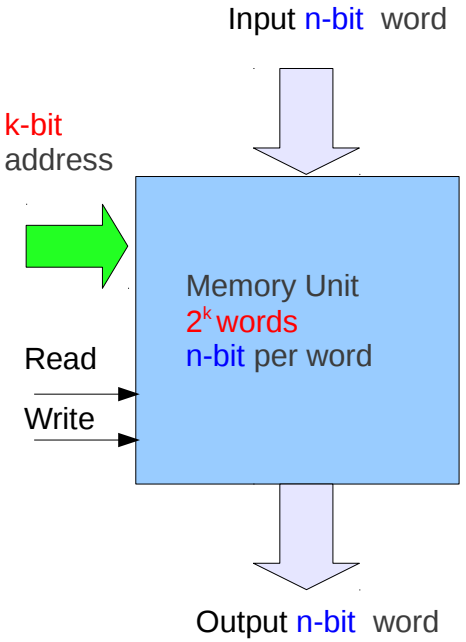


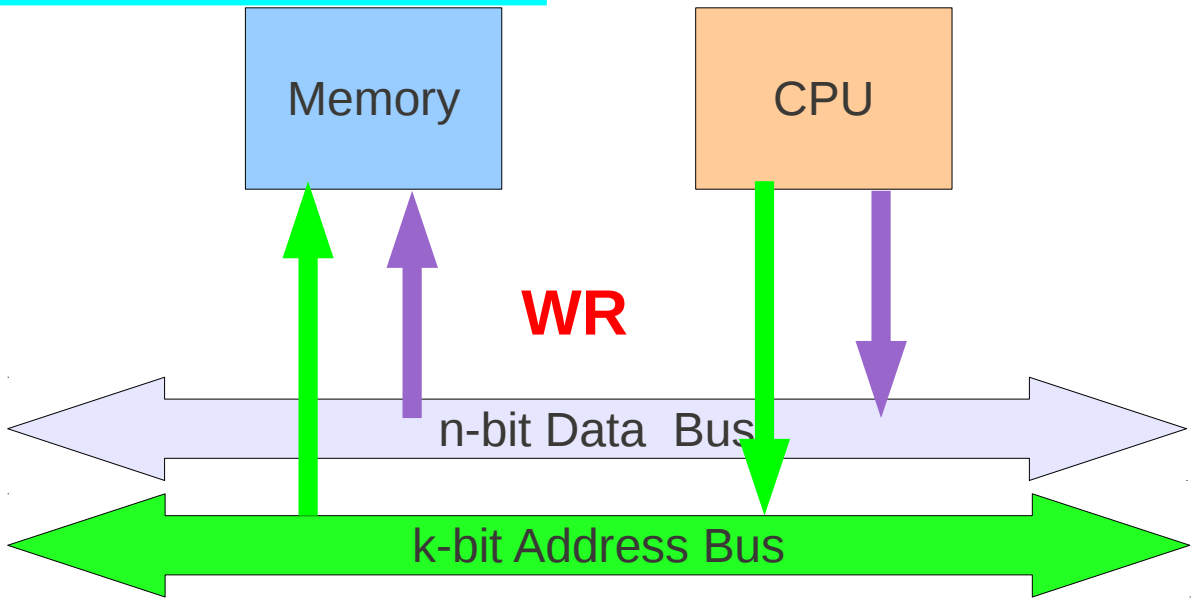


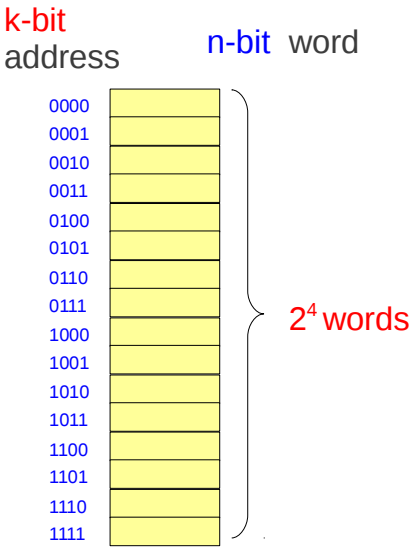


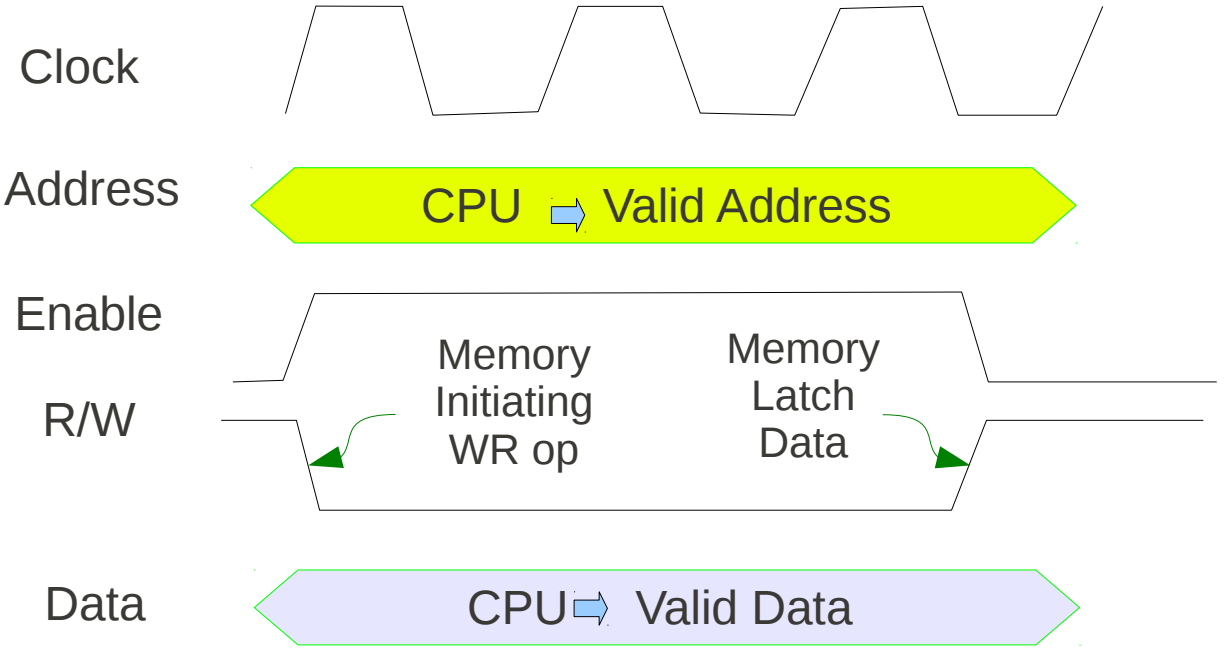


WR Memory Cycle

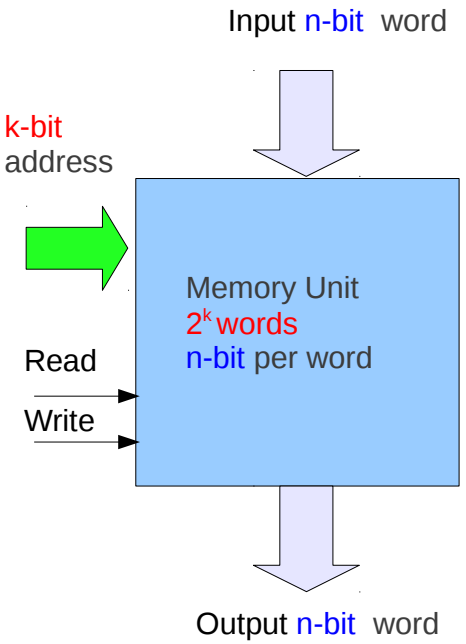


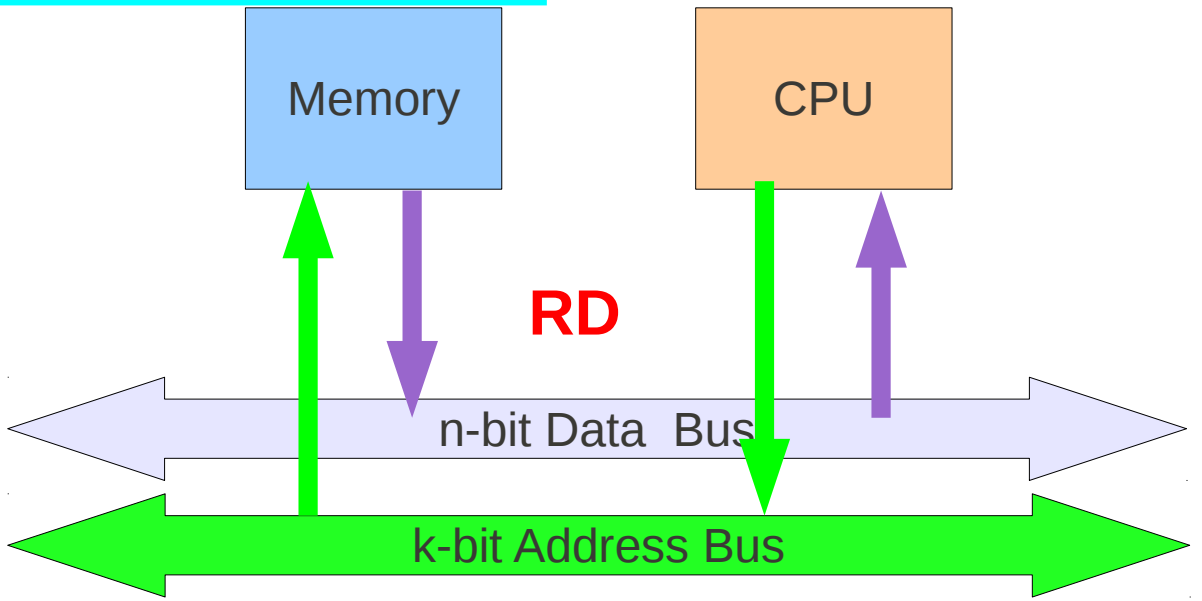


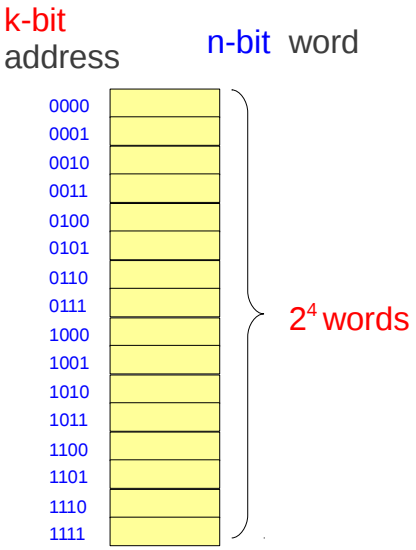


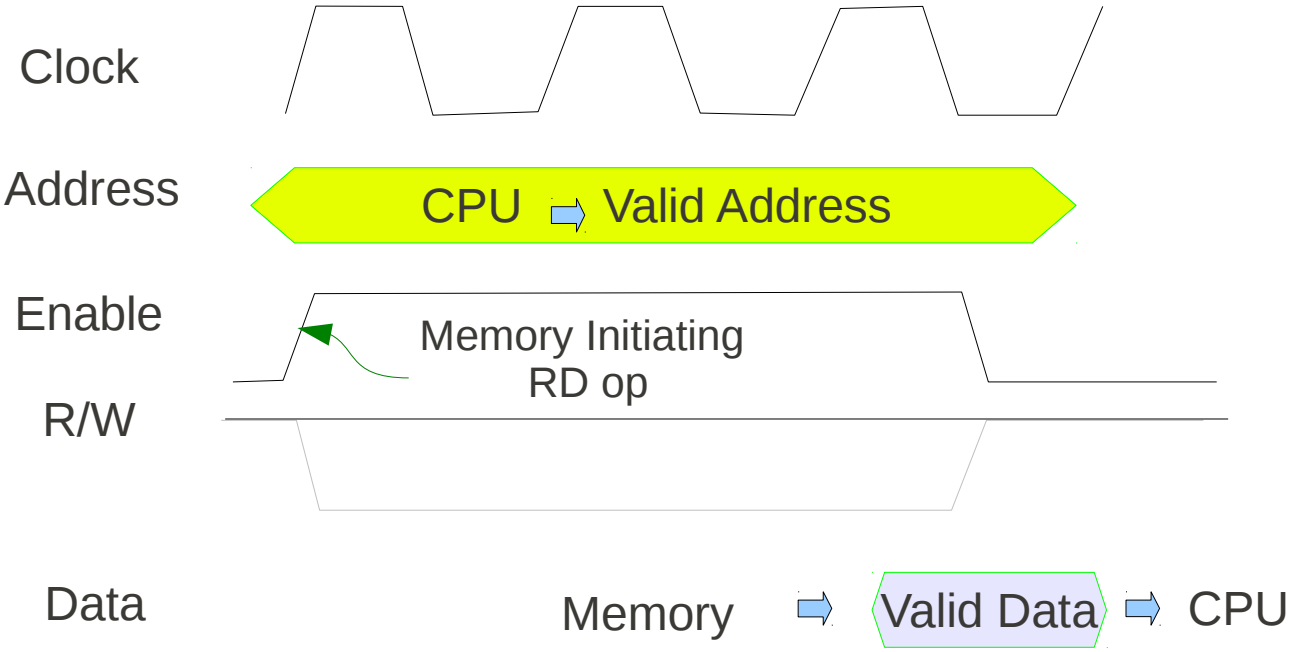


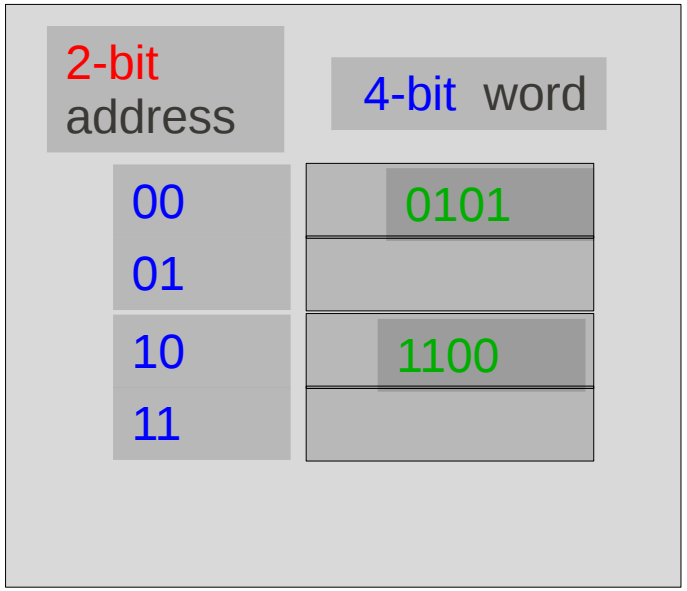
RD Memory Cycle

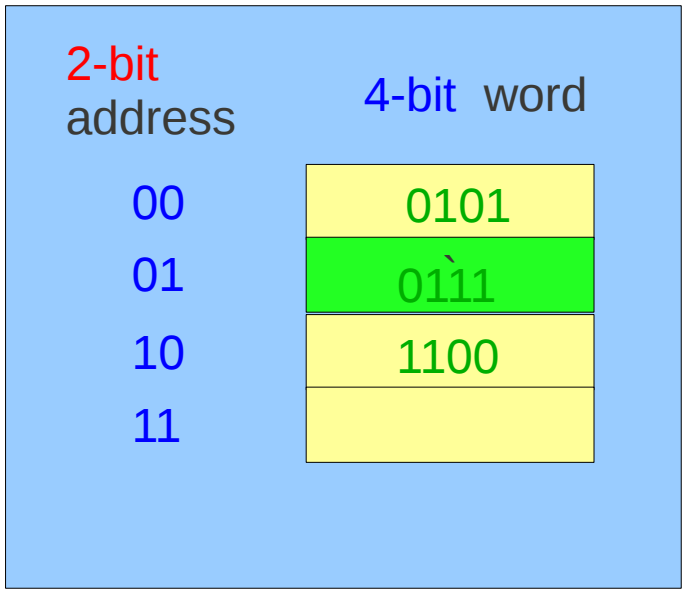






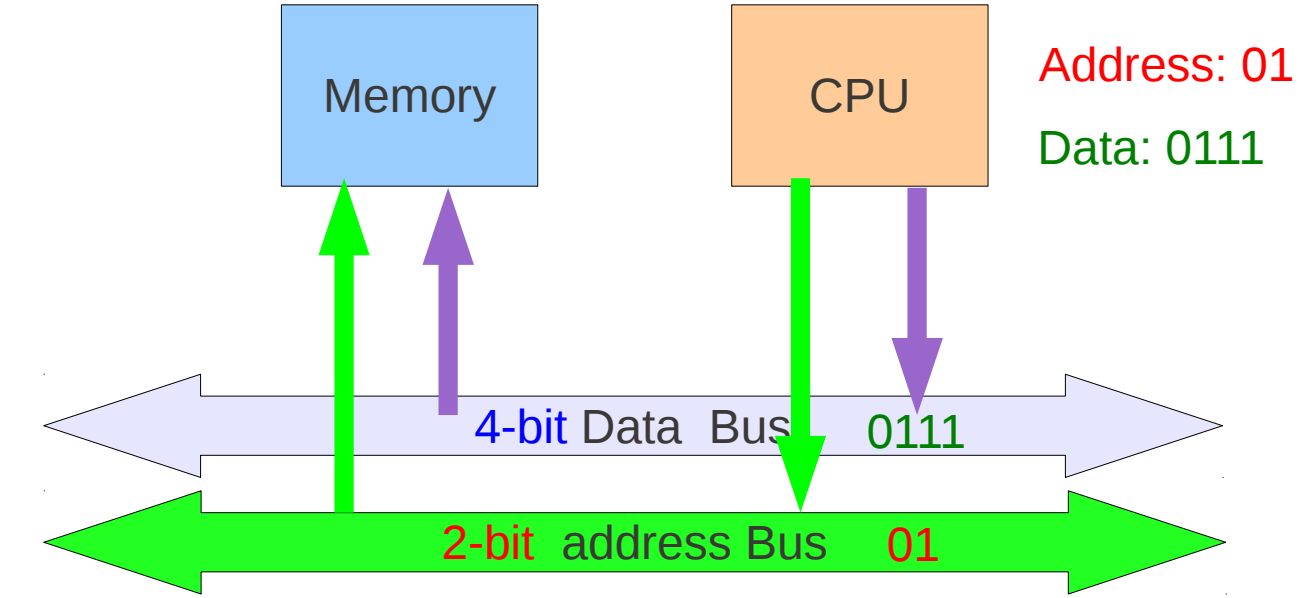


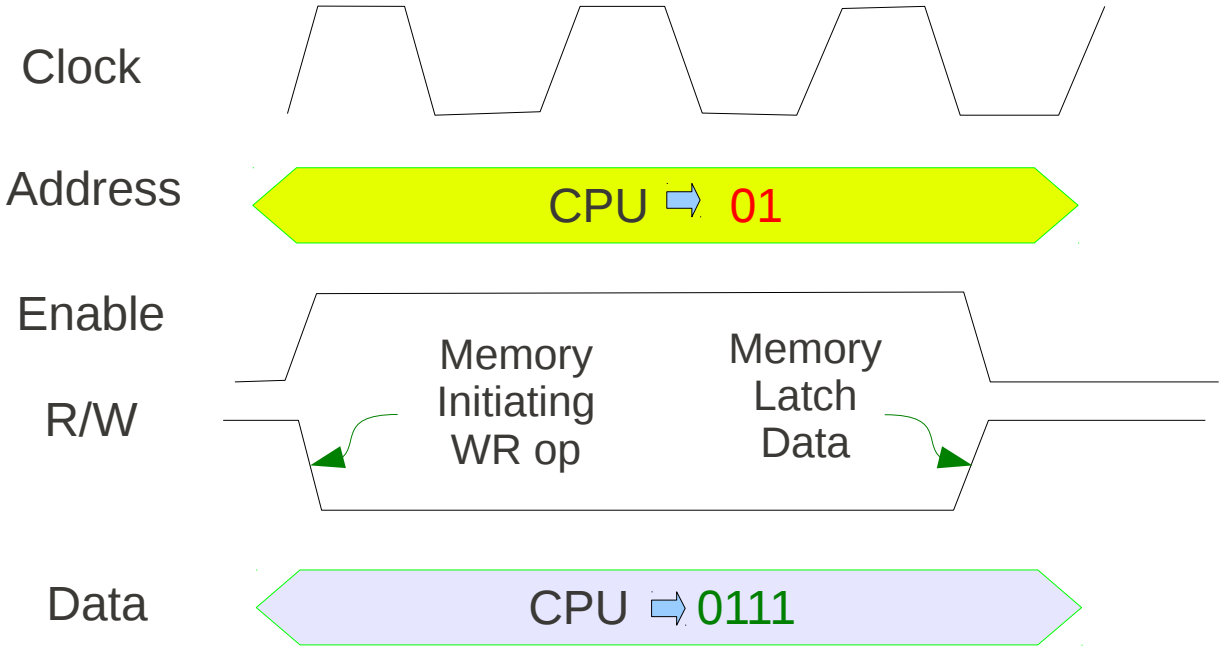


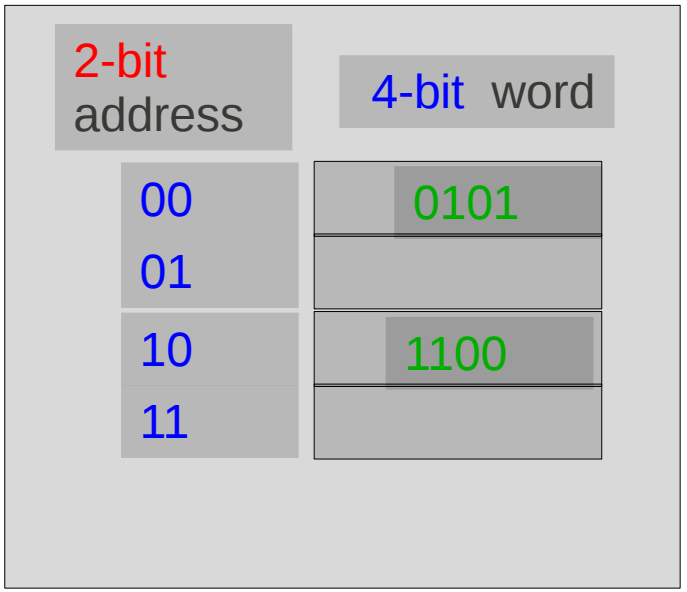


WR Example

WR





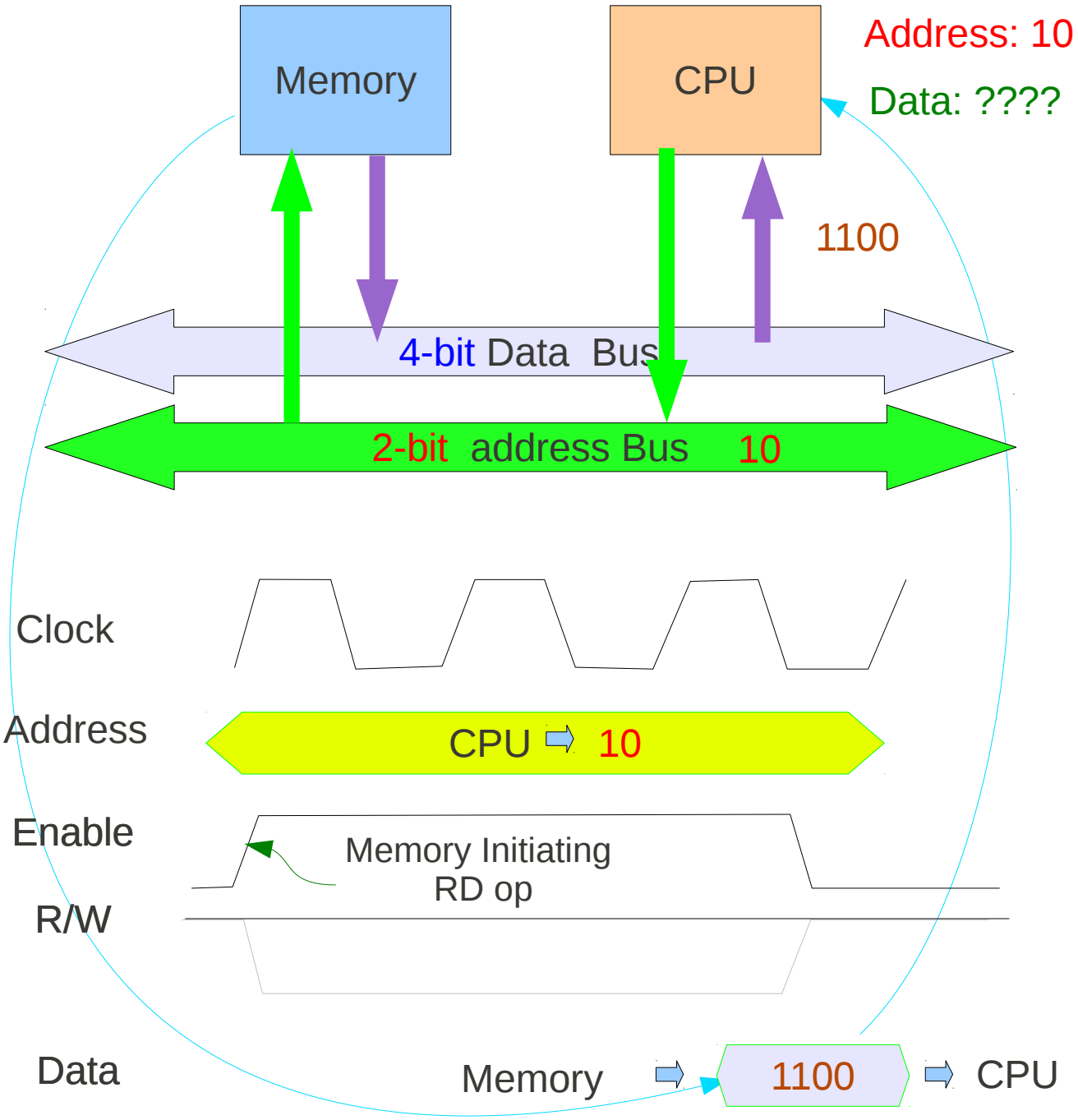


RD Example

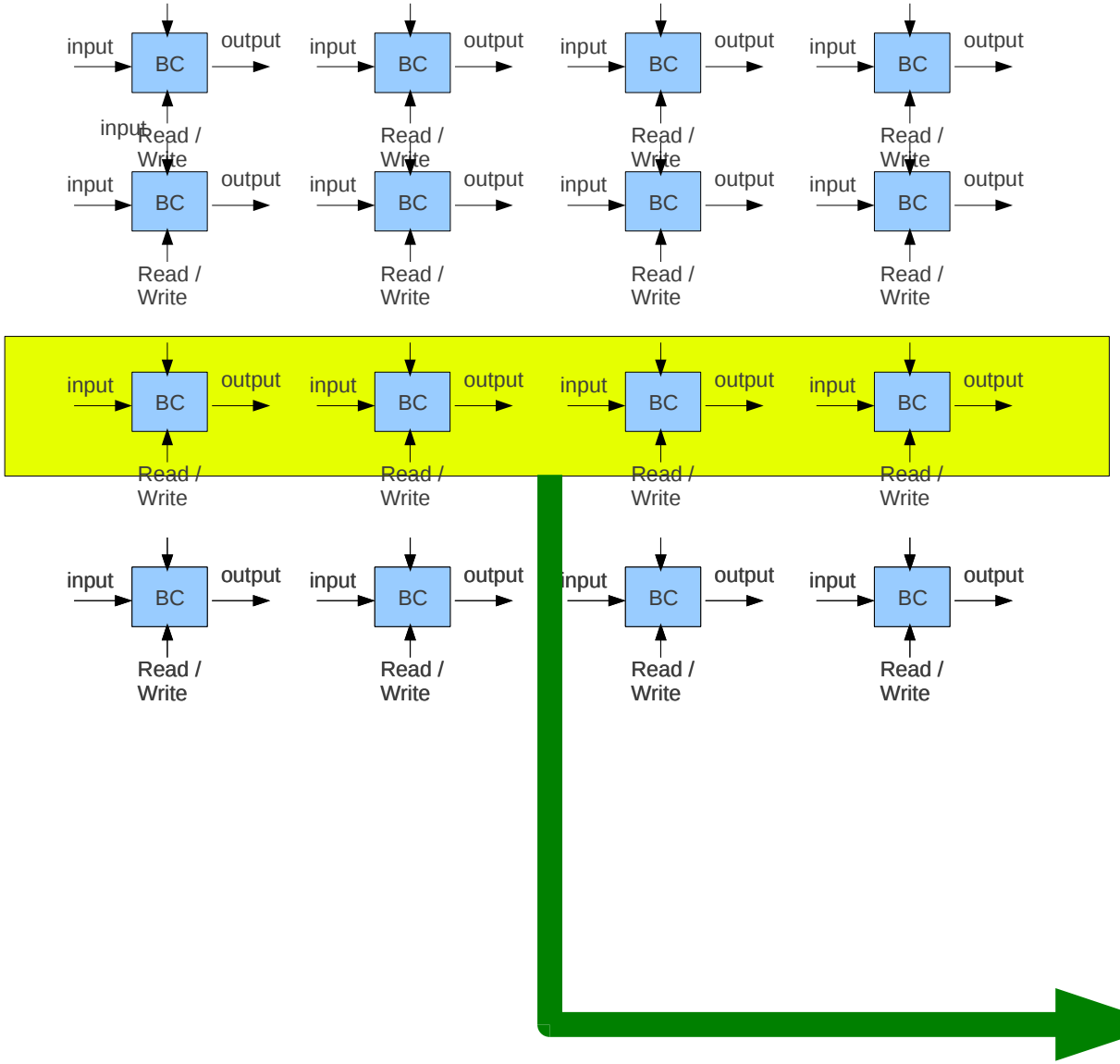
RD

Address: 10

Data: ????



Select A Word



2-bit address

00

01

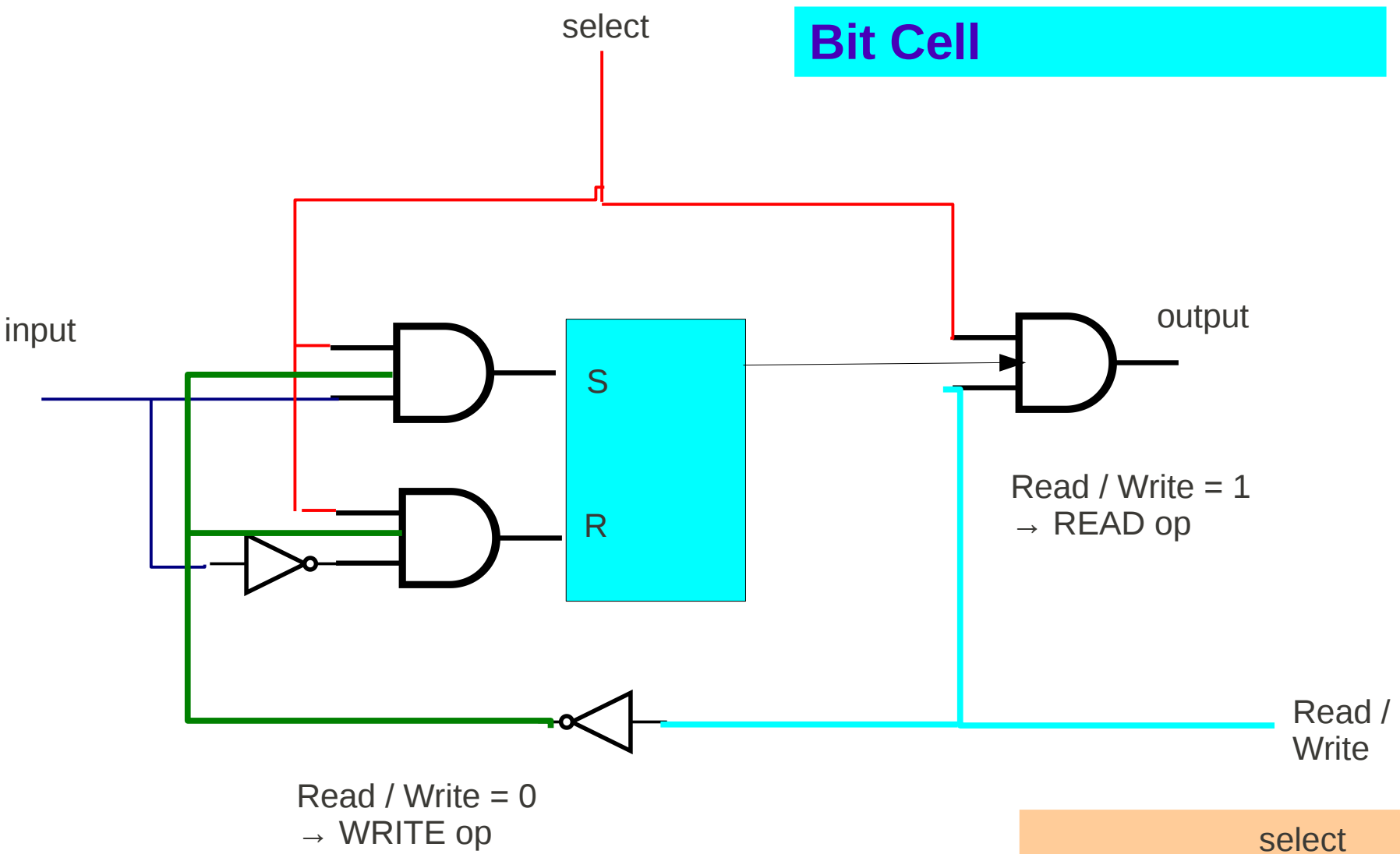
10

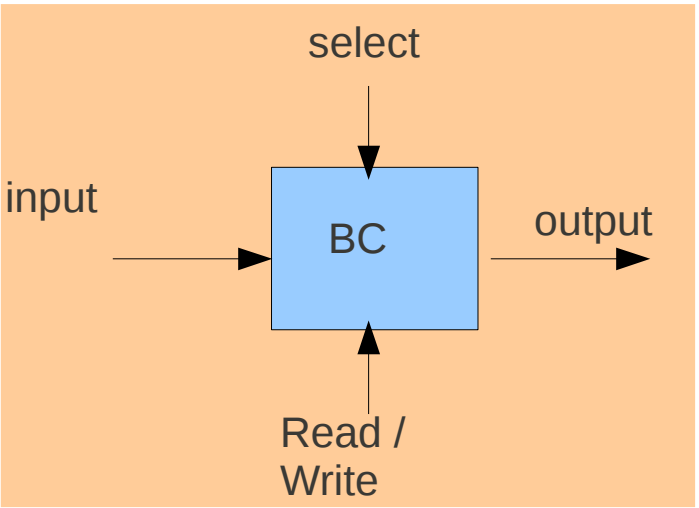
11

4-bit word

2^4 words

Bit Cell

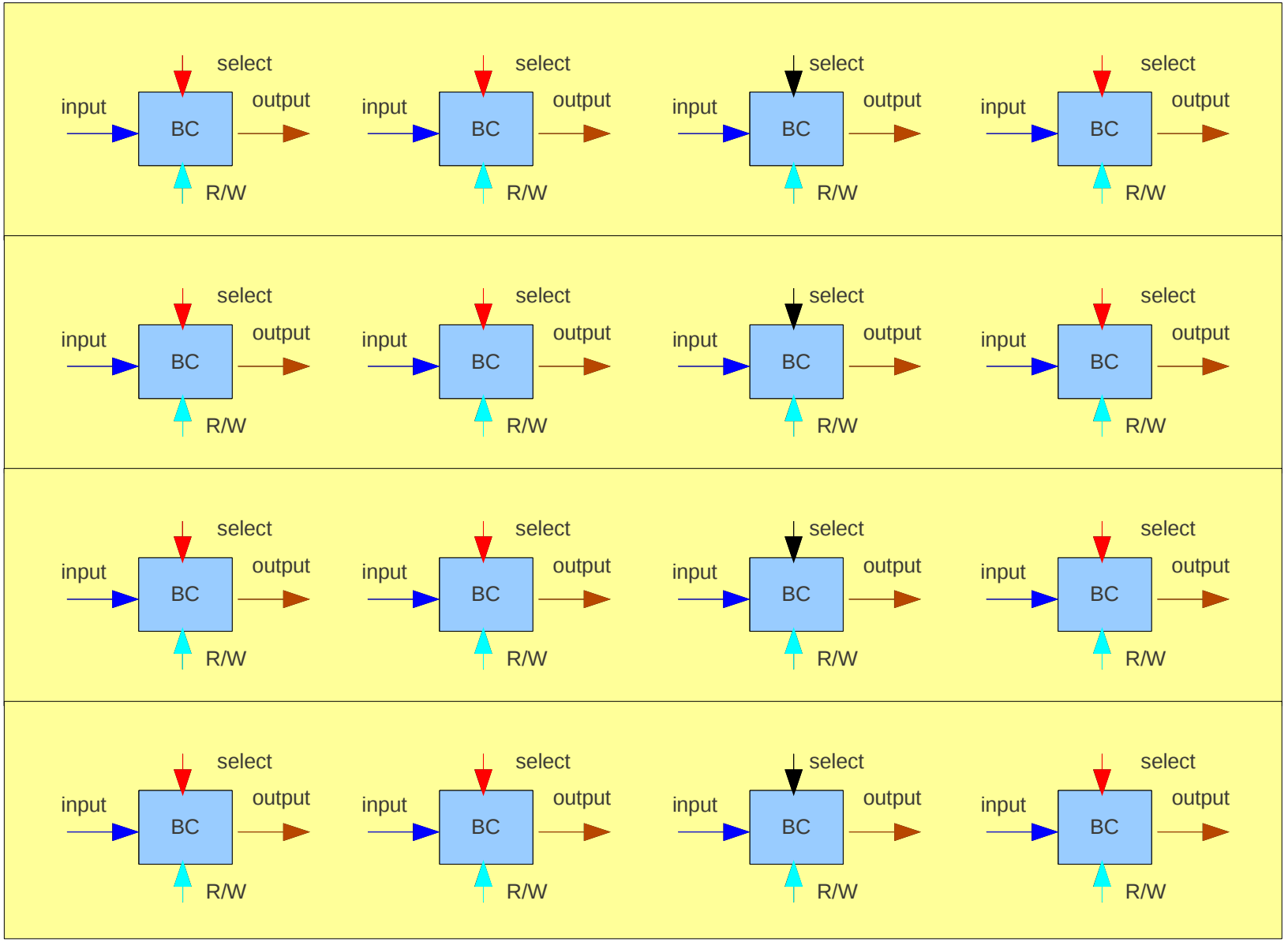

select
input
S
R
output
Read / Write = 1
→ READ op
Read /
Write
Read / Write = 0
→ WRITE op


select
input
BC
output
Read /
Write

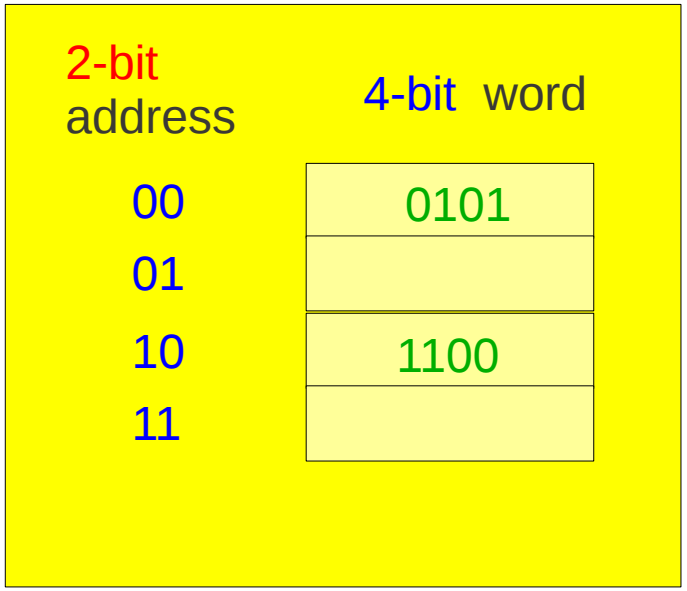
2-bit address

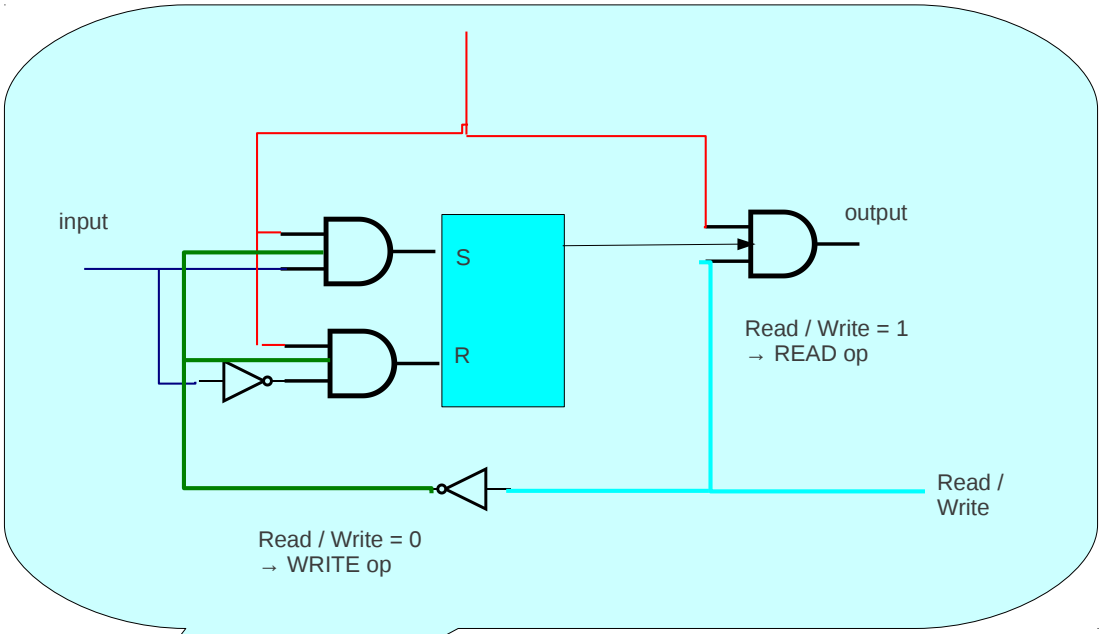
4-bit word

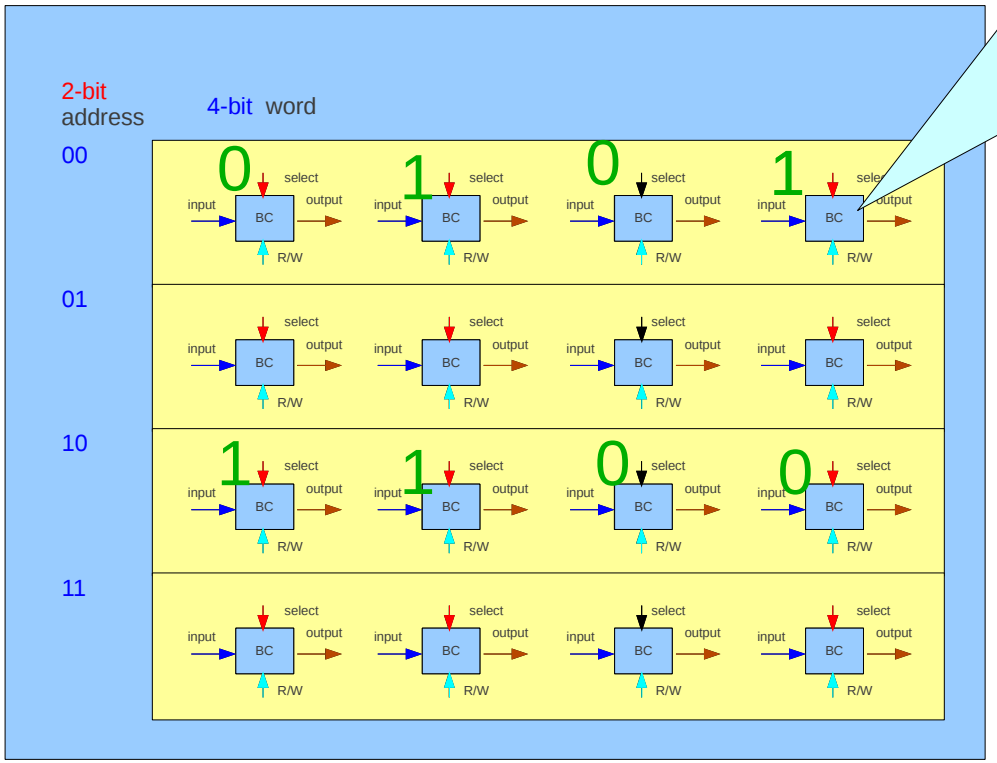
Memory Map

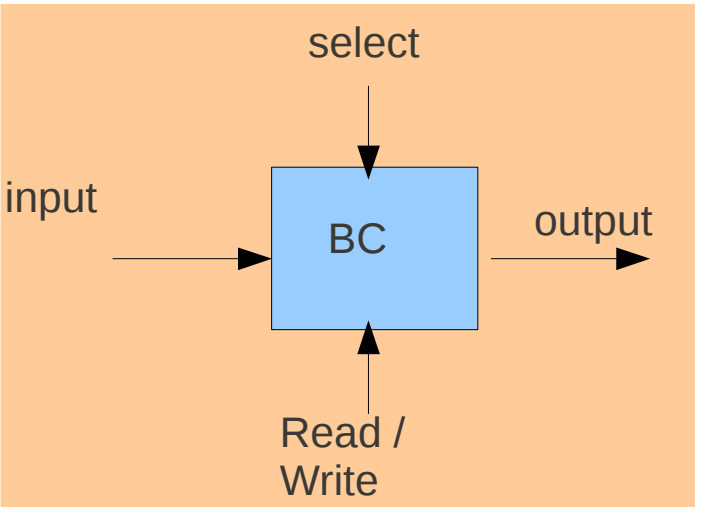


Bit 3 Bit 2 Bit 1 Bit 0

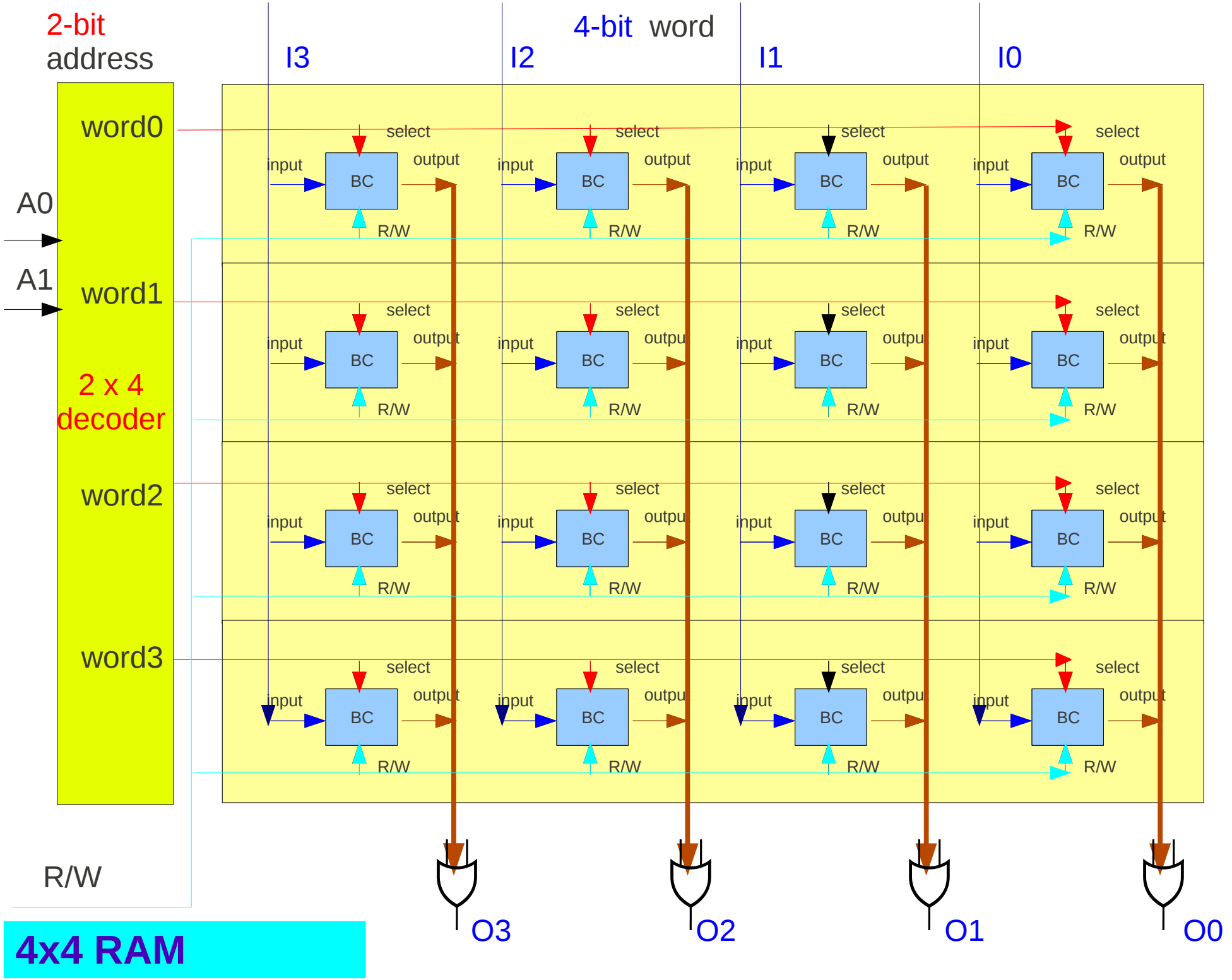

2-bit
address
4-bit word
00
01
10
11
0101
1100

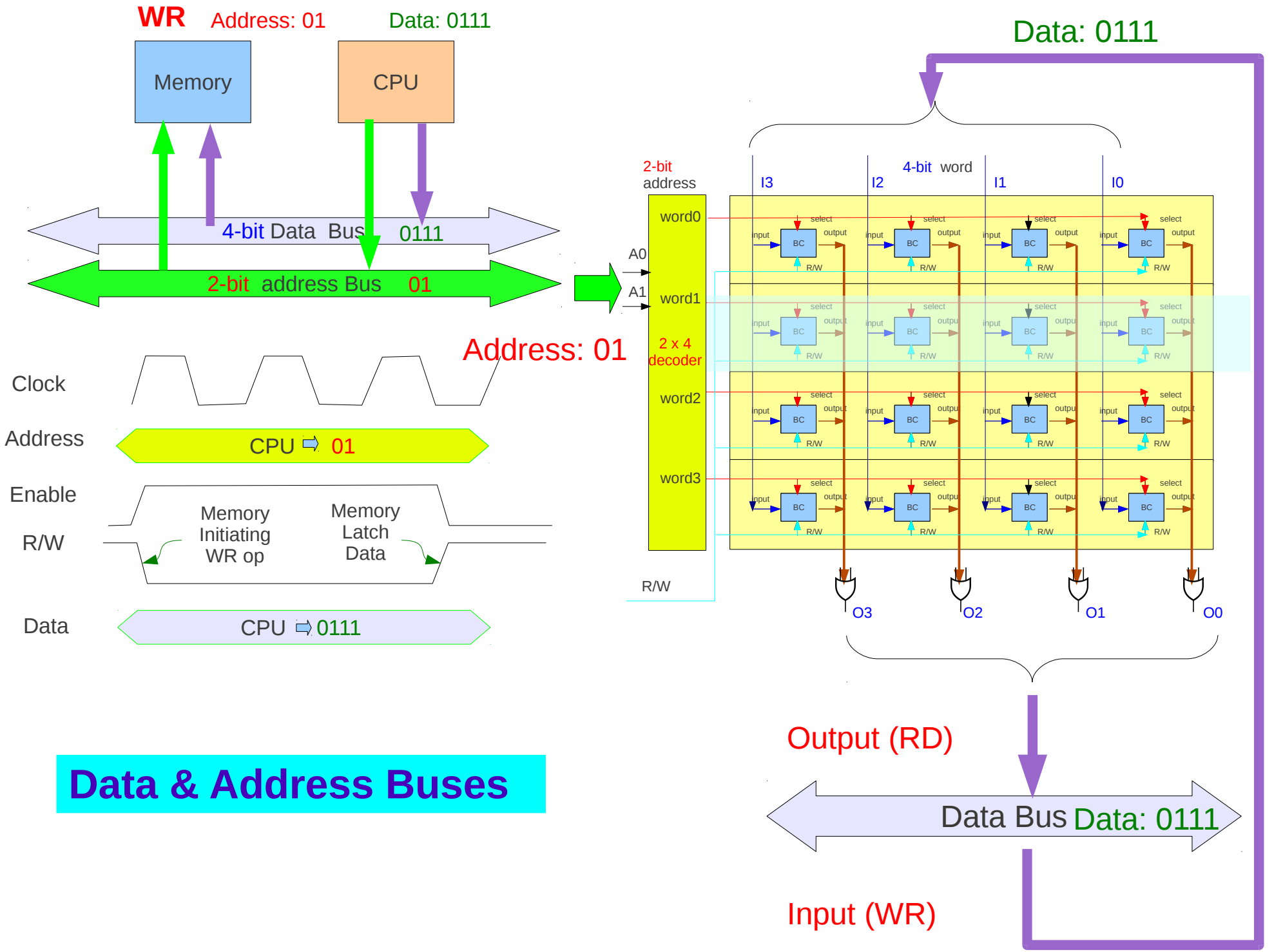

input
S
R
output
Read / Write = 1
→ READ op
Read /
Write
Read / Write = 0
→ WRITE op


2-bit
address
4-bit word
00
01
10
11
select
input
output
BC
R/W

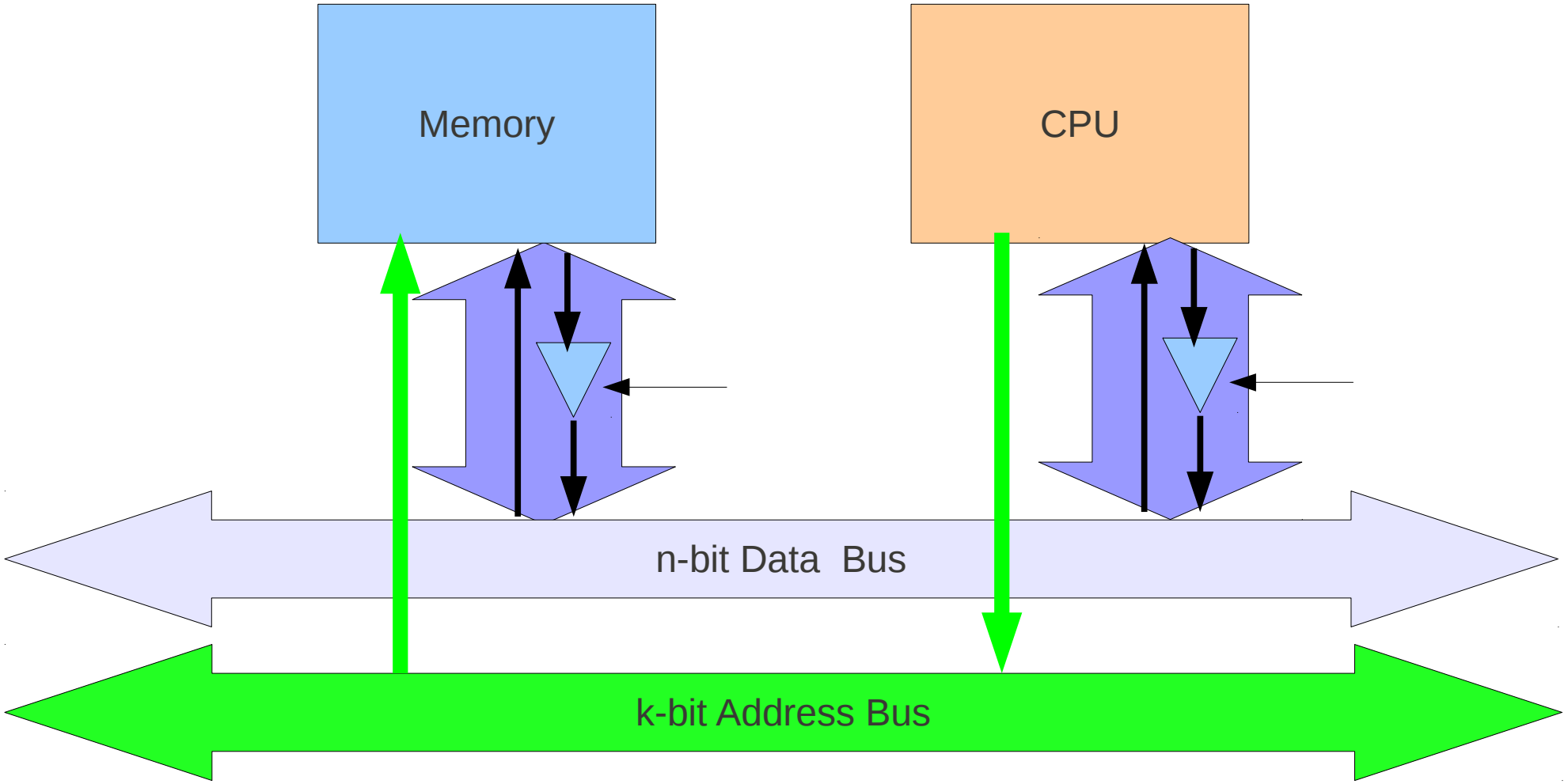

select
input
BC
output
Read /
Write

4x4 RAM

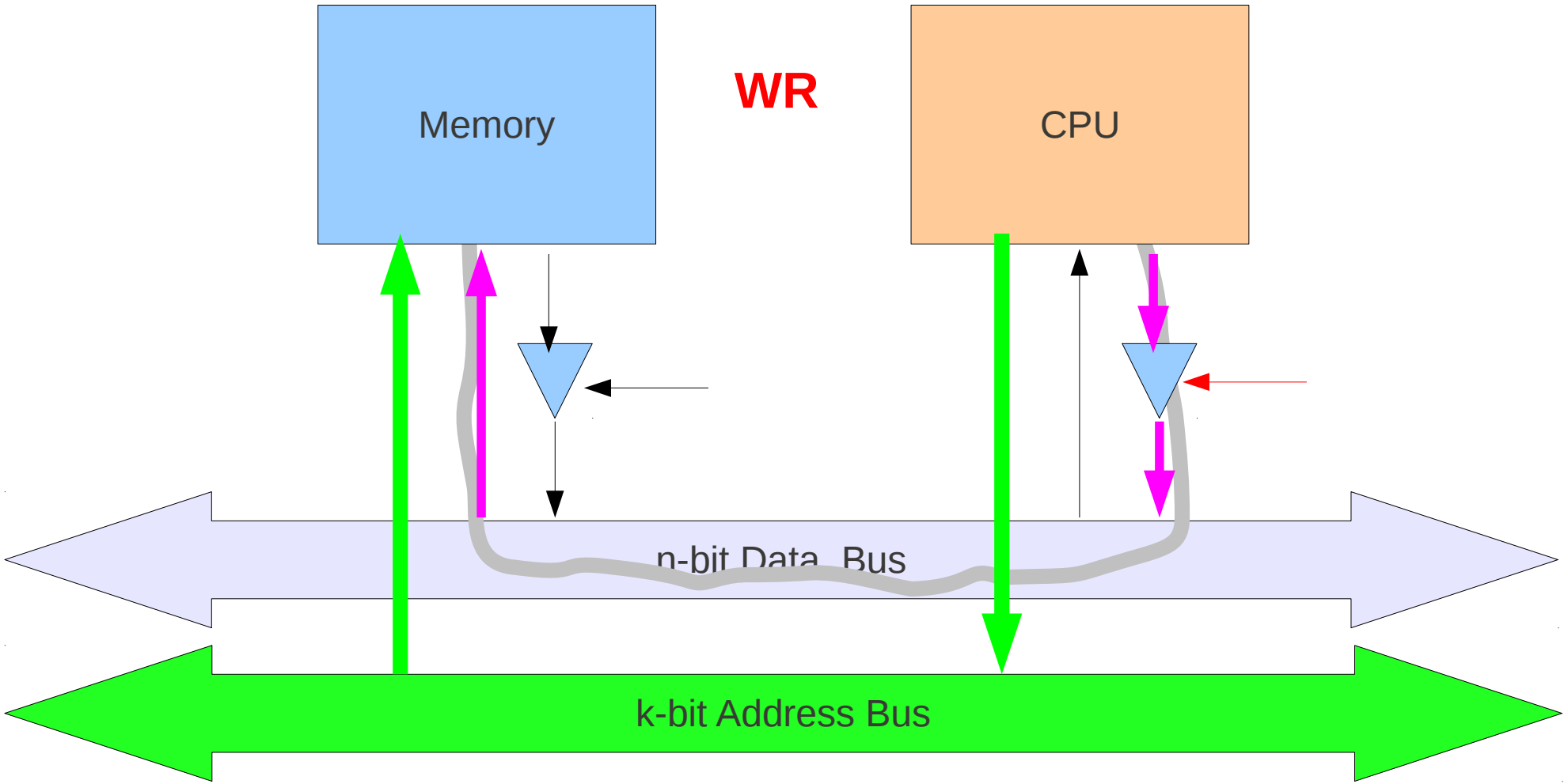

2-bit
address
4-bit word
I3
I2
I1
I0
word0
word1
word2
word3
A0
A1
2 x 4
decoder
R/W
select
input
output
BC
R/W
O3
O2
O1
O0
4x4 RAM


WR
Address: 01
Data: 0111
Memory
CPU
4-bit Data Bus 0111
2-bit address Bus 01
Clock
Address
CPU 01
Enable
R/W
Memory Initiating WR op
Memory Latch Data
Data
CPU 0111
Address: 01
2-bit address
A0
A1
word0
word1
word2
word3
2 x 4 decoder
R/W
4-bit word
I3
I2
I1
I0
select
input
output
BC
R/W
O3
O2
O1
O0
Data: 0111
Output (RD)
Data Bus Data: 0111
Input (WR)
Data & Address Buses

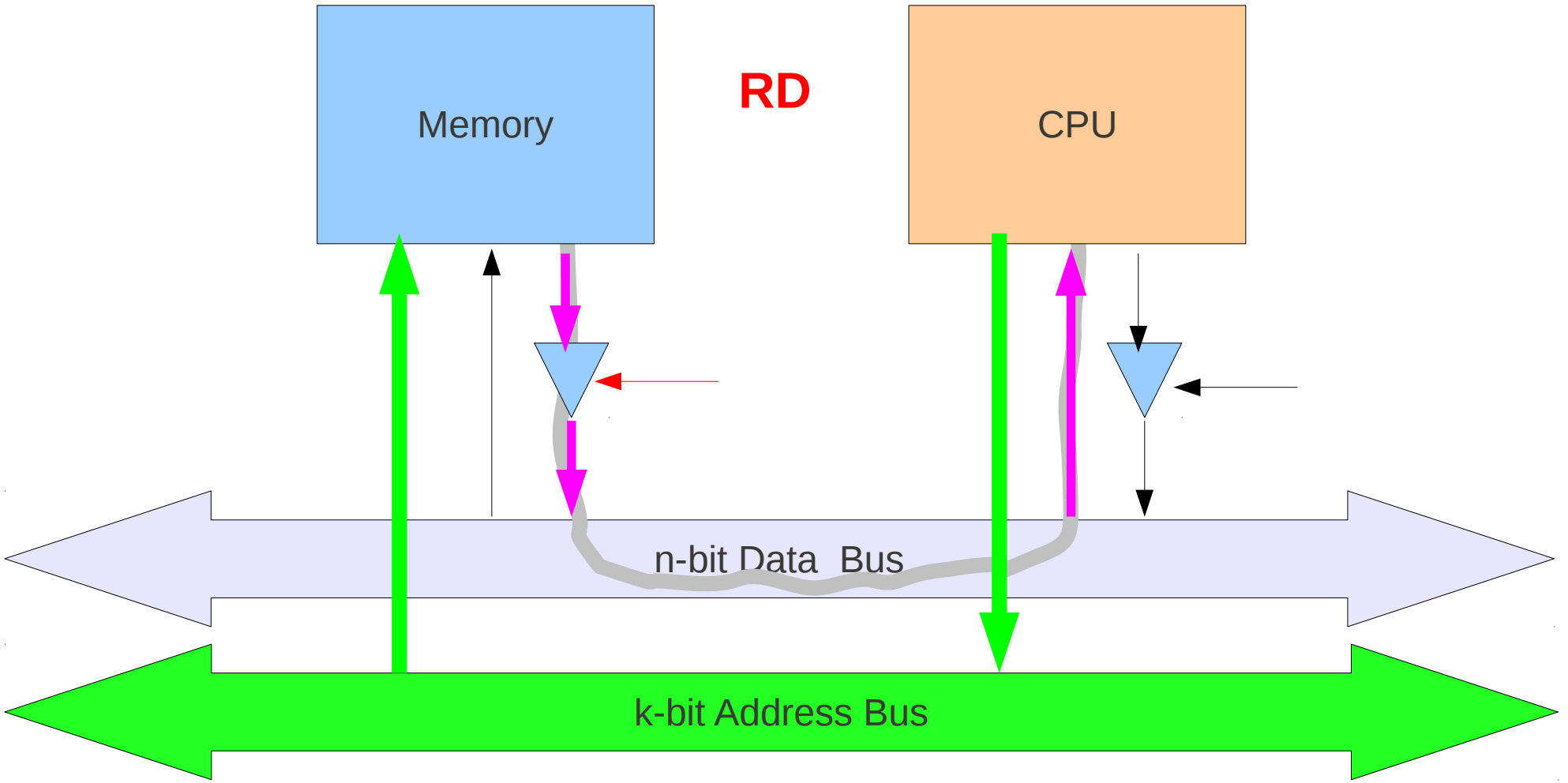
Bi-directional Data Bus



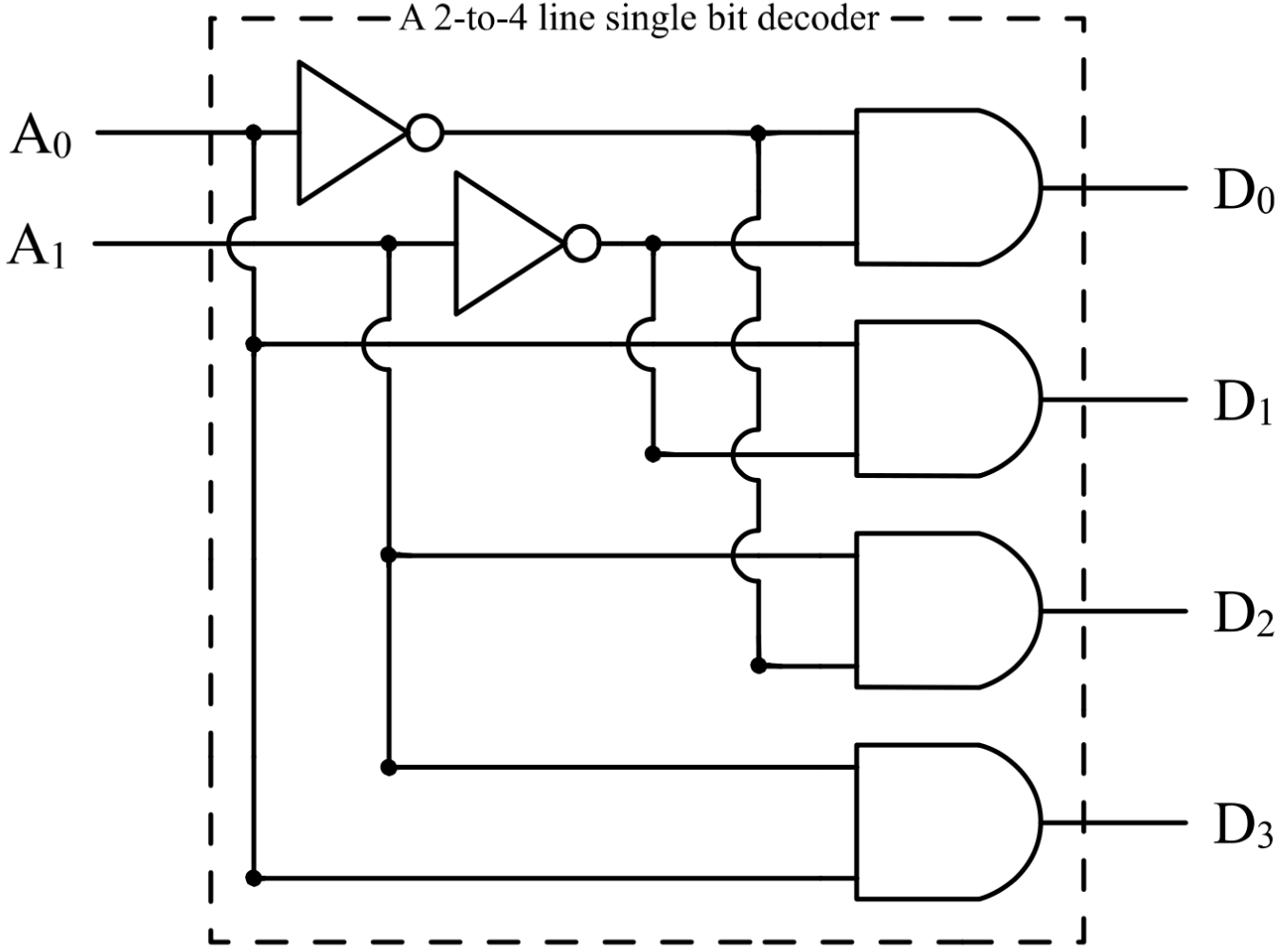
From CPU to Memory



From Memory to CPU



2x4 Decoder



Truth Table

A_1	A_0	D_3	D_2	D_1	D_0
0	0	0	0	0	1
0	1	0	0	1	0
1	0	0	1	0	0
1	1	1	0	0	0

Minterm Equations

$$D_0 = \overline{A_1} \cdot \overline{A_0}$$

$$D_1 = \overline{A_1} \cdot A_0$$

$$D_2 = A_1 \cdot \overline{A_0}$$

$$D_3 = A_1 \cdot A_0$$

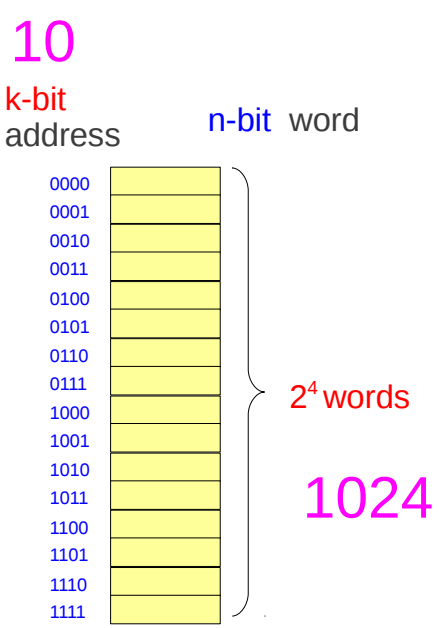
2 x 4 decoder : 4 AND gates

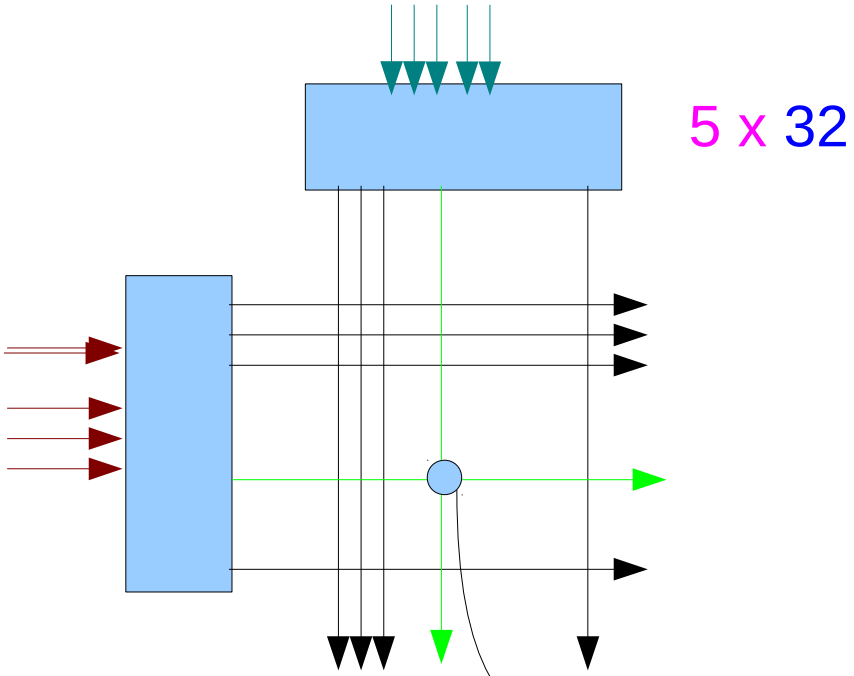
10 x 1024 decoder : 1024 AND gates

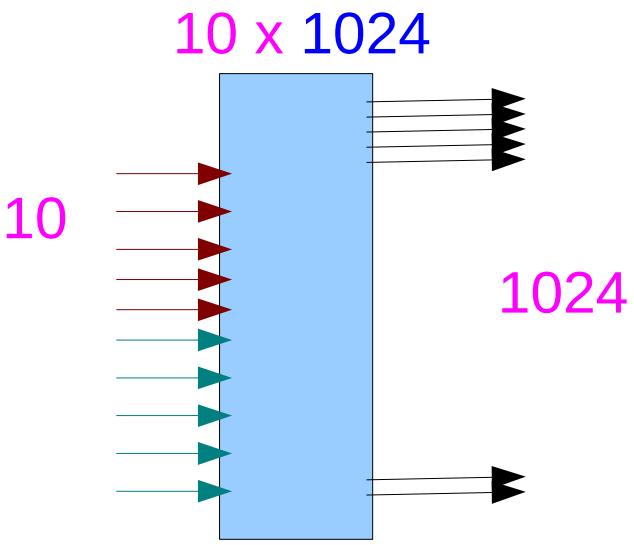
4 x 16 decoder : 16 AND gates

Row and Col Address Decoder

10 x 1024 decoder : 1024 AND gates



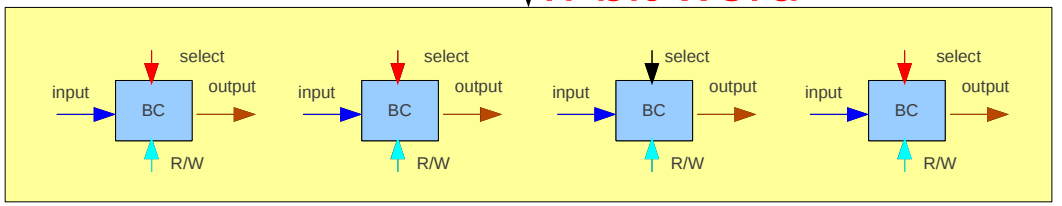




5 x 32

404 → 01100 10110

n-bit word



Time Sharing Address Bus