Edge Triggered Flip Flop

Please send corrections (or suggestions) to youngwlim@hotmail.com.

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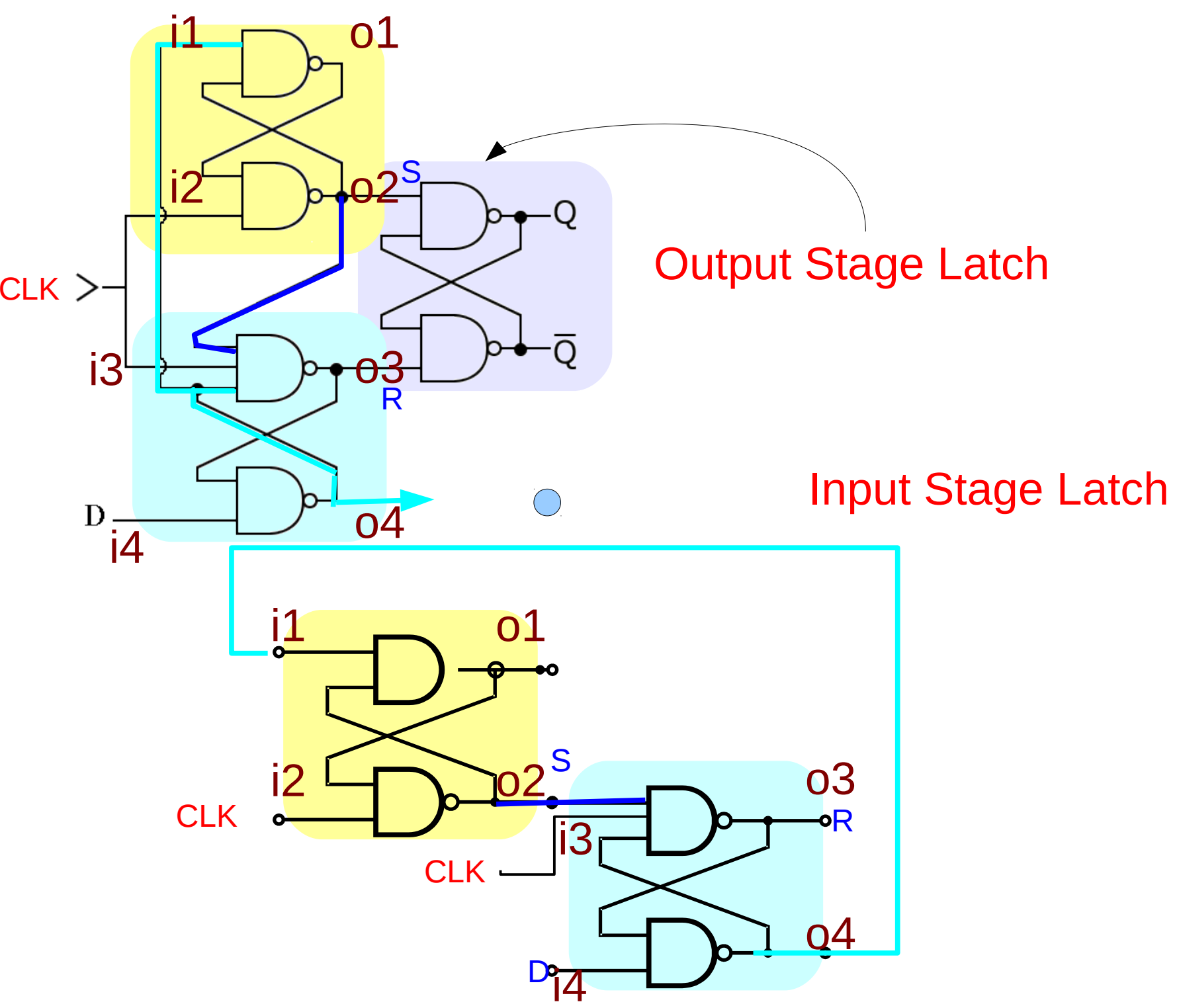
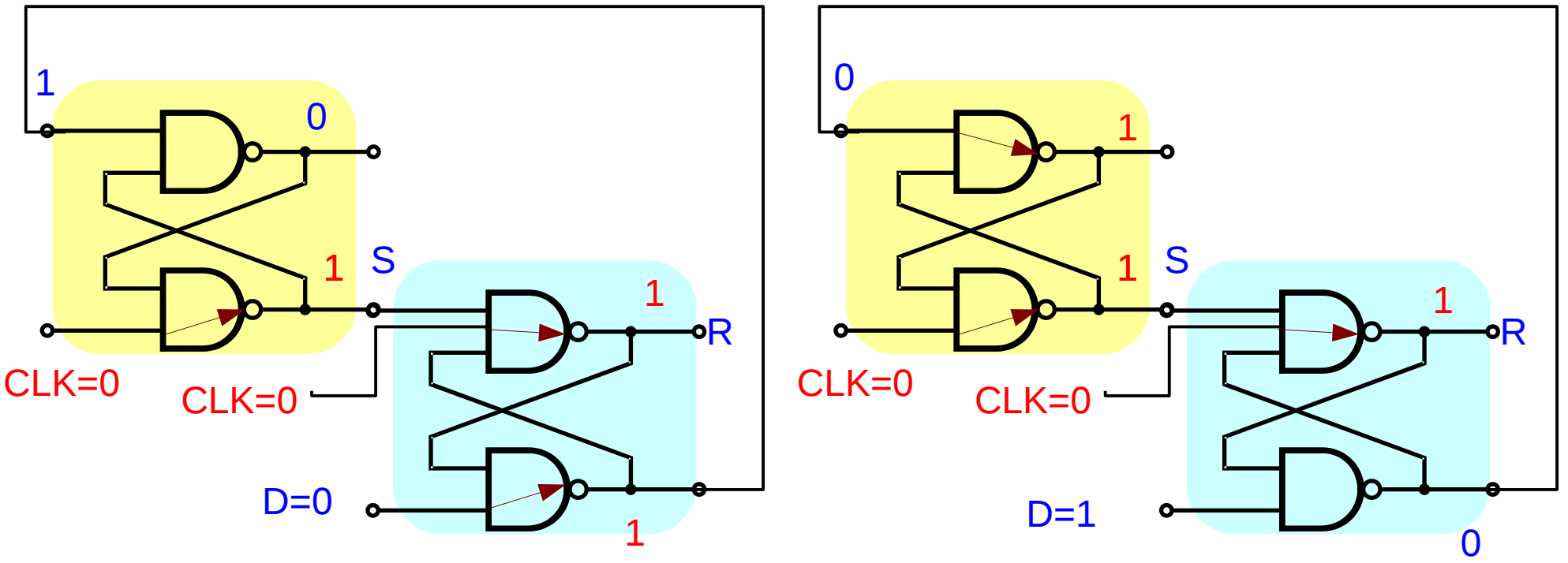

i1
o1
i2
o2
S
Q
CLK
Output Stage Latch
i3
o3
R
D
i4
o4
Input Stage Latch
i1
o1
i2
o2
S
o3
CLK
R
i3
CLK
o4
D
i4

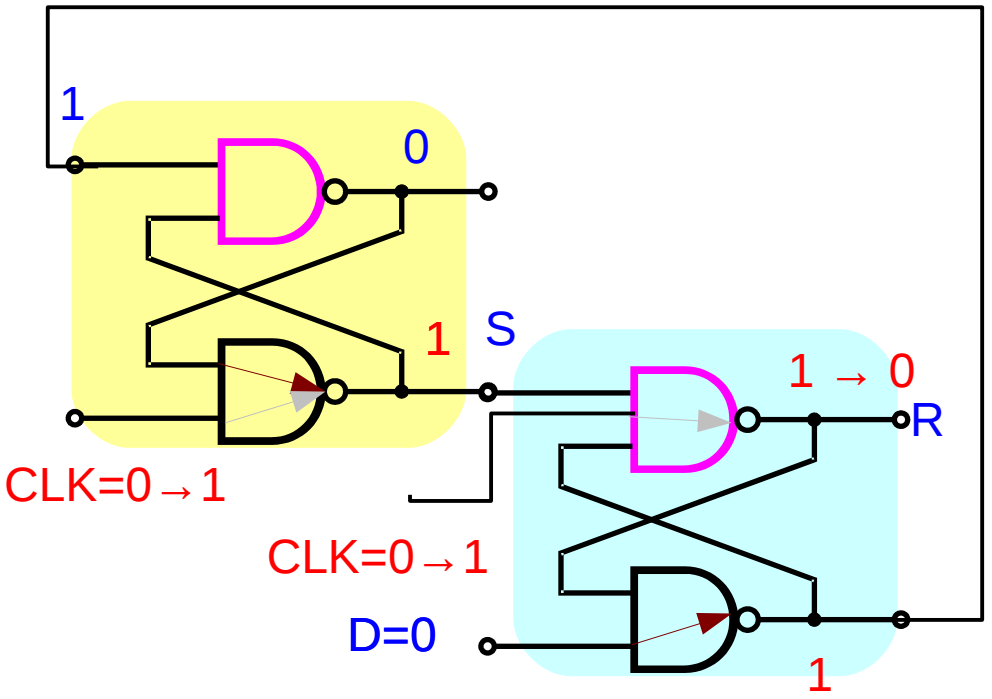
Input Stage Latch – CLK =0 SR=11

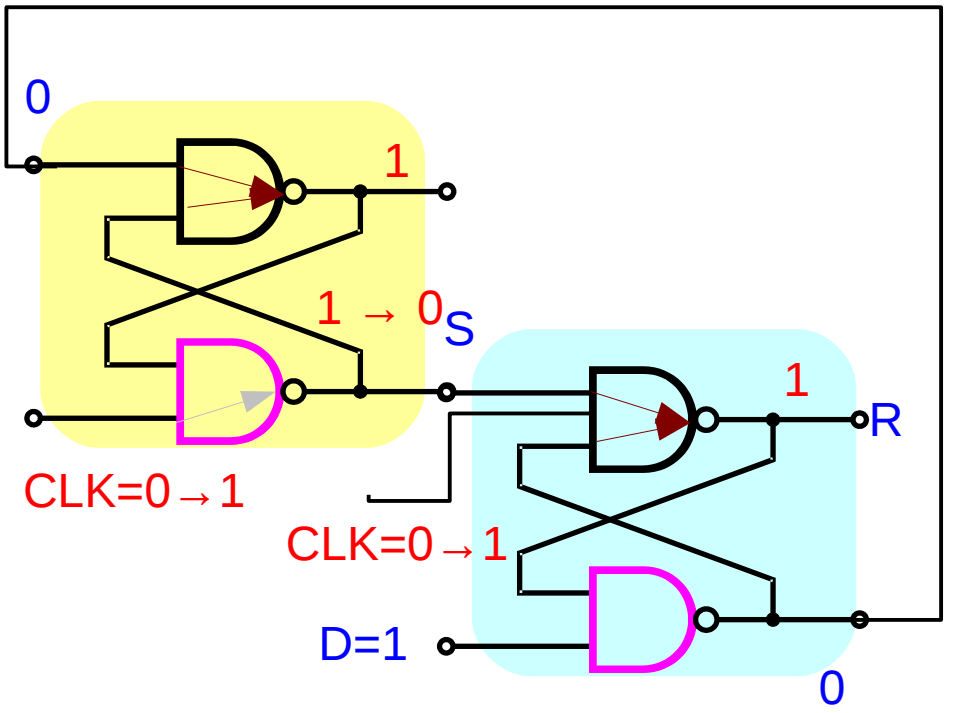


If the clock is low,
both the output signals of the input stage are high
regardless of the data input;
the output latch is unaffected and it stores the
previous state.

Input Stage Latch – Rising Edge

D=0 → SR=10
D=1 → SR=01

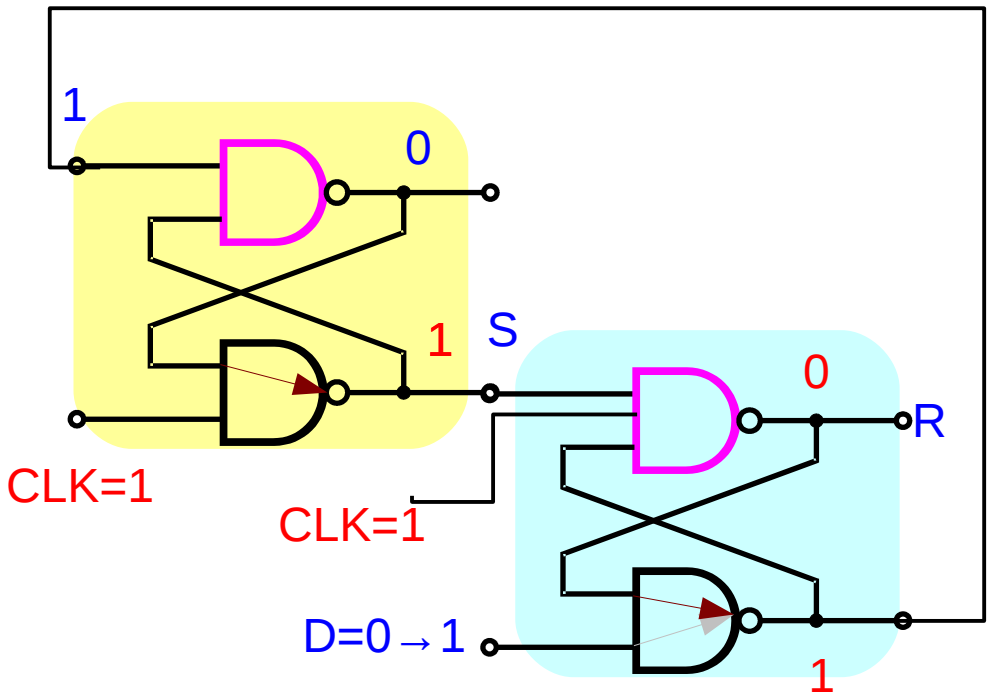


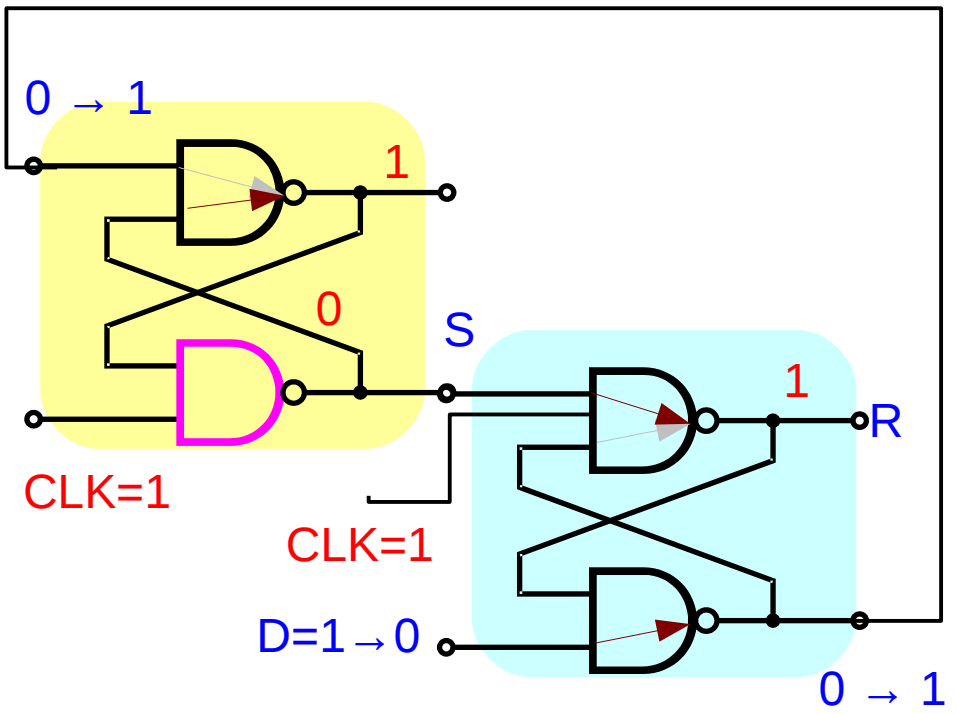


When the clock signal changes from low to high,
only one of the output voltages (S or R) goes low
(depending on the data signal D)
SR = 01 or SR = 10
and sets/resets the output latch:
if D = 0, the lower output becomes low ; (Reset operation SR=10)
if D = 1, the upper output becomes low. (Set operation SR=01)

Input Stage Latch – CLK=1

D=(0 → 1) → SR=10
D=(1 → 0) → SR=01





If the clock signal continues staying **high**,
the outputs keep their states (D=0: SR=10, D=1: SR=01)
regardless of the data input
and force the output latch to stay in the corresponding state
as the input logical zero remains active (SR=10: Reset, SR=01: Set)
while the clock is **high**.

The input stage (the two latches on the left)
processes the clock and data signals
to ensure correct input signals
for the output stage (the single latch on the right).

If the clock is low,
both the output signals of the input stage are high
regardless of the data input;
the output latch is unaffected and it stores the previous state.

If the clock signal continues staying high,

the outputs keep their states

regardless of the data input

and force the output latch to stay in the corresponding state

as the input logical zero remains active

while the clock is high.

Hence the role of the output latch is to store the data only while the clock is low.

The circuit is closely related to the gated D latch as both the circuits convert the two D input states (0 and 1) to two input combinations (01 and 10) for the output SR latch by inverting the data input signal (both the circuits split the single D signal in two complementary S and R signals).

The difference is that in the gated D latch simple NAND logical gates are used while in the positive-edge-triggered D flip-flop SR NAND latches are used for this purpose. The role of these latches is to "lock" the active output producing low voltage (a logical zero); thus the positive-edge-triggered D flip-flop can be thought of as a gated D latch with latched input gates.

References

[1] http://en.wikipedia.org/