

# Structure (1A)

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- Component

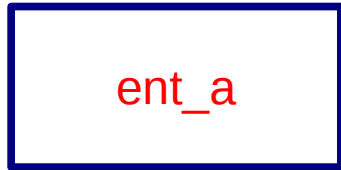
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# Entity and Architecture

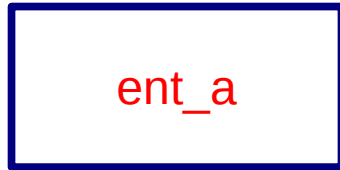


```
entity ent_a is  
    port ( ... );  
end ent_a;
```

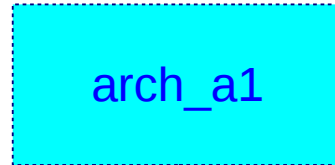


```
architecture arch_a of ent_a is  
    port ( ... );  
end ent_a;
```

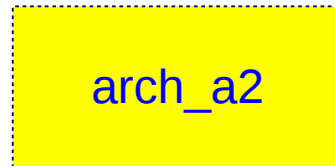
# Many Architectures



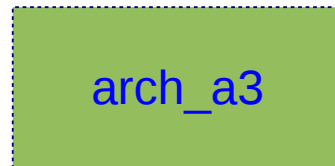
```
entity ent_a is  
    port ( ... );  
end ent_a;
```



```
architecture arch_a1 of ent_a is  
    ...  
end ent_a;
```

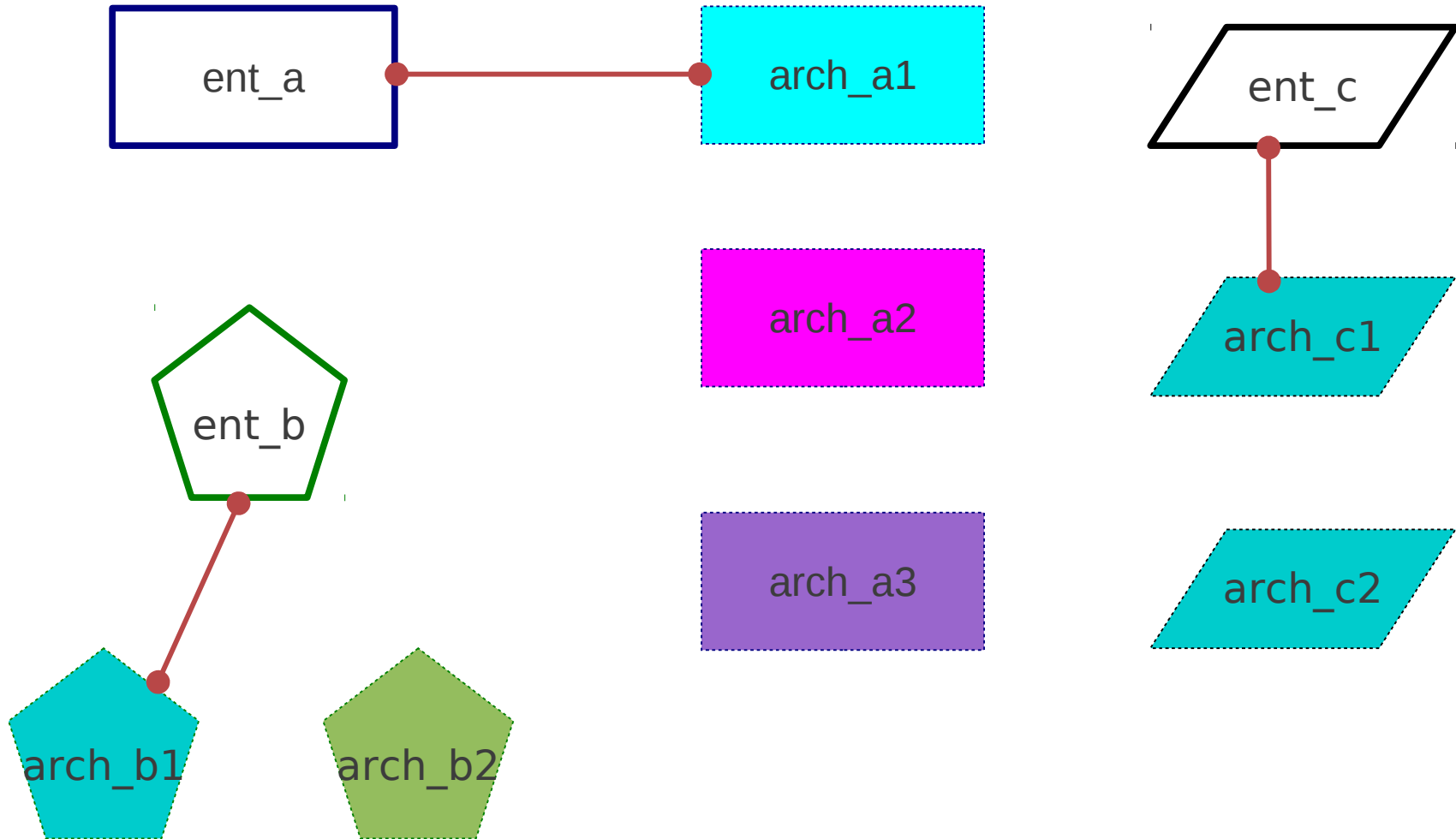


```
architecture arch_a2 of ent_a is  
    ...  
end ent_a;
```

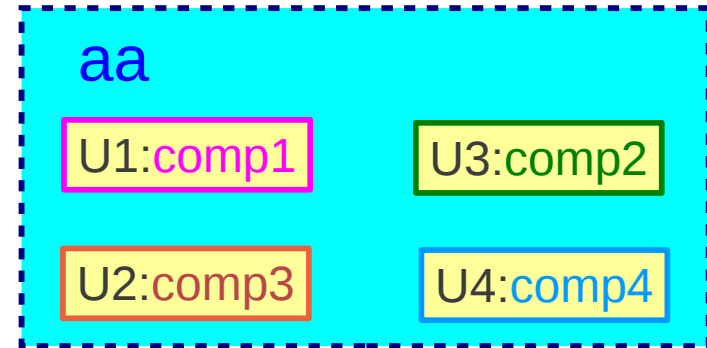


```
architecture arch_a3 of ent_a is  
    ...  
end ent_a;
```

# Entity - Architecture Binding



# Sequential Assignment (2)



## Component Declaration

```
component comp1 is
  port ( );
end comp1;
component comp2 is
  port ( );
end comp2;
component comp3 is
  port ( );
end comp3;
component comp4 is
  port ( );
end comp4;
```

## architecture aa of ee is

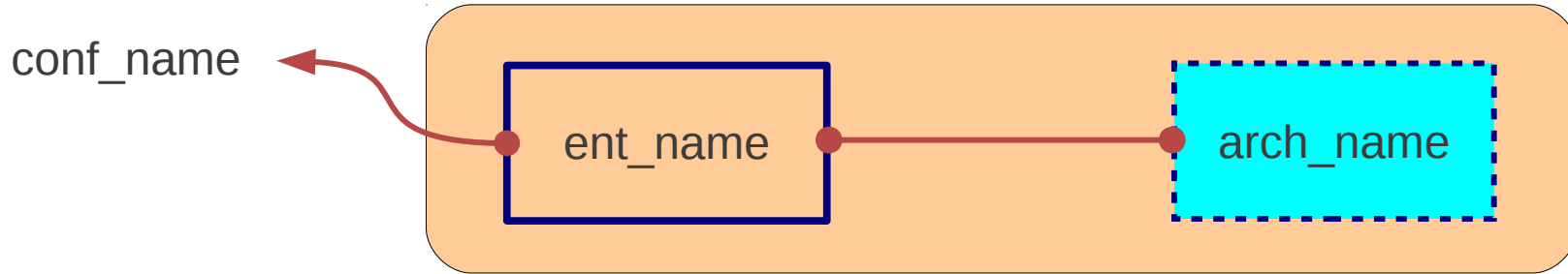
begin

## Component Instantiation

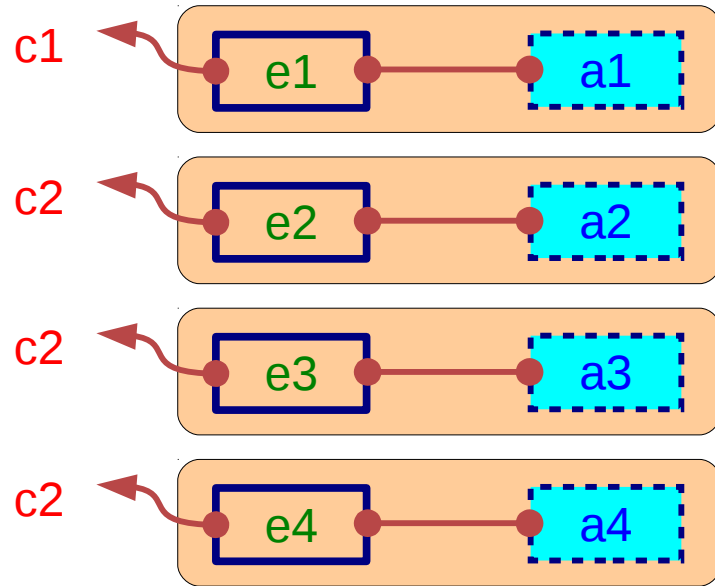
```
U1: comp1 port map ( );
U2: comp2 port map ( );
U3: comp3 port map ( );
U4: comp4 port map ( );
```

end aa;

# Configuration

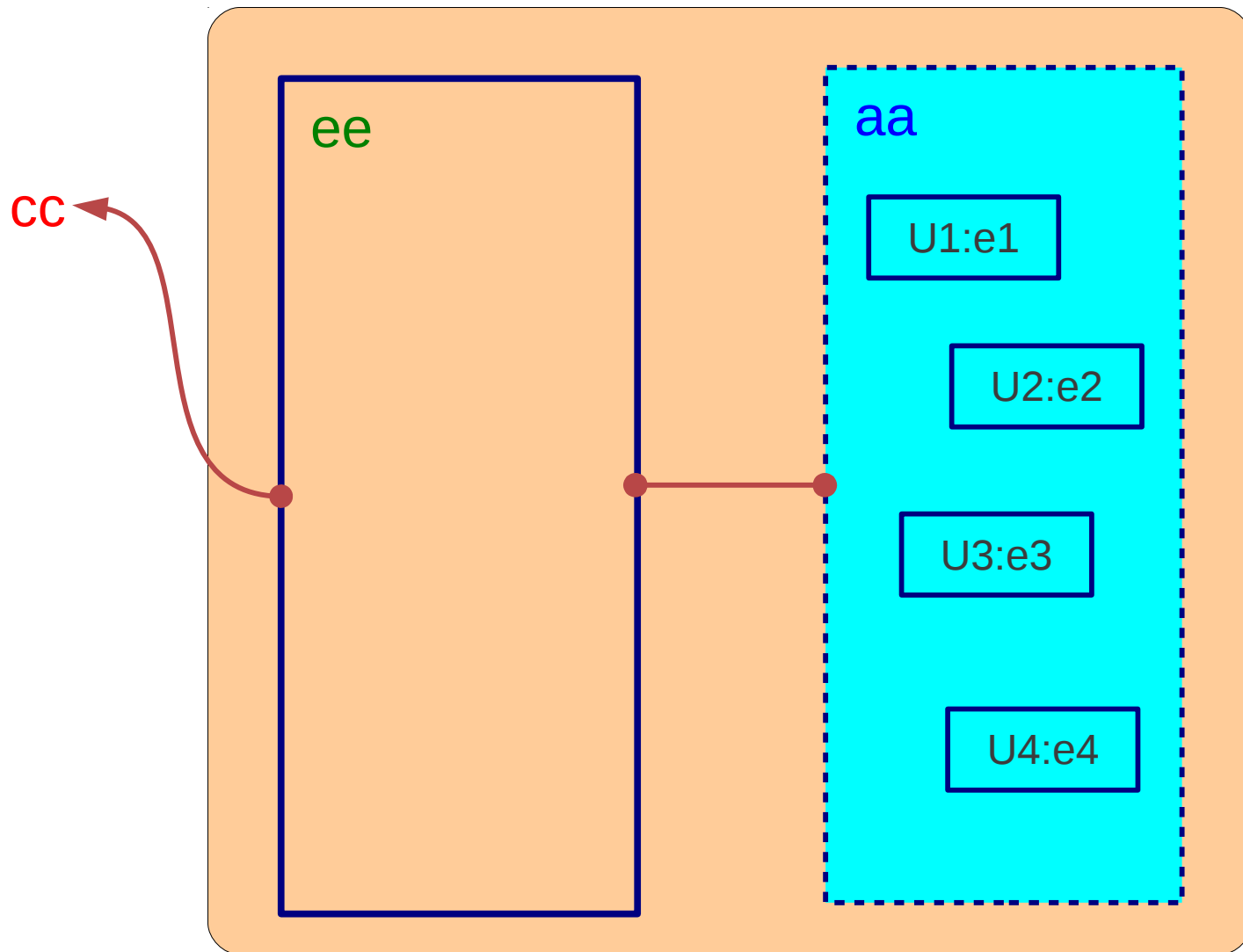


# Configuration

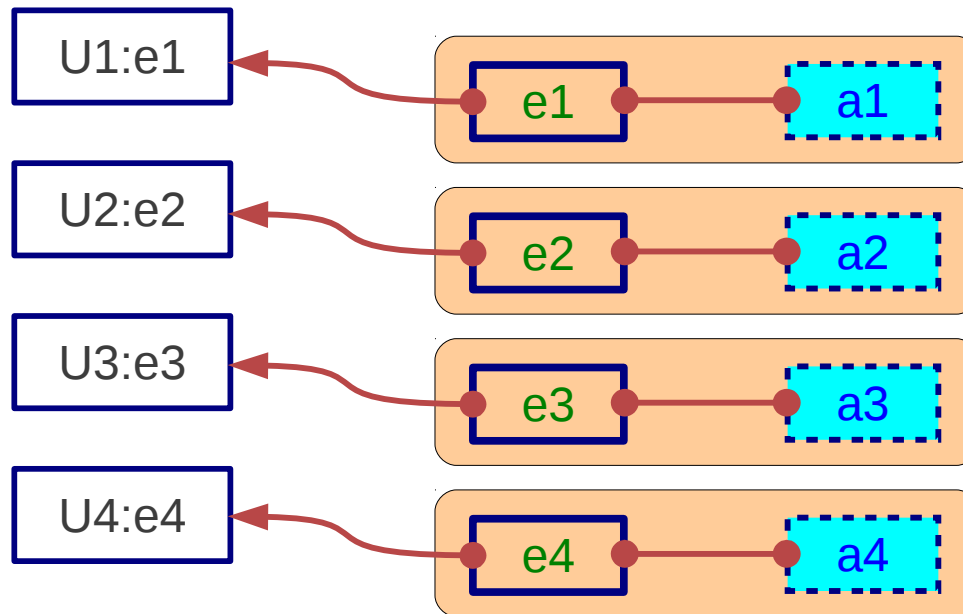




# Sequential Assignment (2)



# Sequential Assignment (2)



## References

- [1] <http://en.wikipedia.org/>
- [2] J. V. Spiegel, VHDL Tutorial,  
[http://www.seas.upenn.edu/~ese171/vhdl/vhdl\\_primer.html](http://www.seas.upenn.edu/~ese171/vhdl/vhdl_primer.html)
- [3] J. R. Armstrong, F. G. Gray, Structured Logic Design with VHDL
- [4] Z. Navabi, VHDL Analysis and Modeling of Digital Systems
- [5] D. Smith, HDL Chip Design
- [6] <http://www.csee.umbc.edu/portal/help/VHDL/stdpkg.html>
- [7] VHDL Tutorial - VHDL online [www.vhdl-online.de/tutorial/](http://www.vhdl-online.de/tutorial/)