

Configuration (1A)

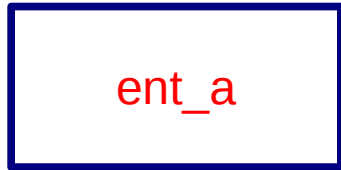
Copyright (c) 2012 Young W. Lim.

Permission is granted to copy, distribute and/or modify this document under the terms of the GNU Free Documentation License, Version 1.2 or any later version published by the Free Software Foundation; with no Invariant Sections, no Front-Cover Texts, and no Back-Cover Texts. A copy of the license is included in the section entitled "GNU Free Documentation License".

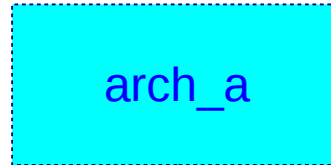
Please send corrections (or suggestions) to youngwlim@hotmail.com.

This document was produced by using OpenOffice and Octave.

Sequential Assignment (1)

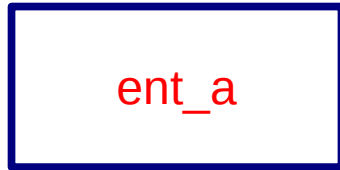


```
entity ent_a is  
    port ( ... );  
end ent_a;
```

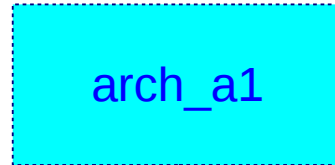


```
architecture arch_a of ent_a is  
    port ( ... );  
end ent_a;
```

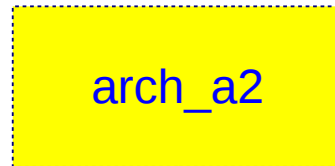
Sequential Assignment (1)



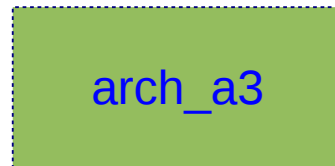
```
entity ent_a is  
    port ( ... );  
end ent_a;
```



```
architecture arch_a1 of ent_a is  
    port ( ... );  
end ent_a;
```

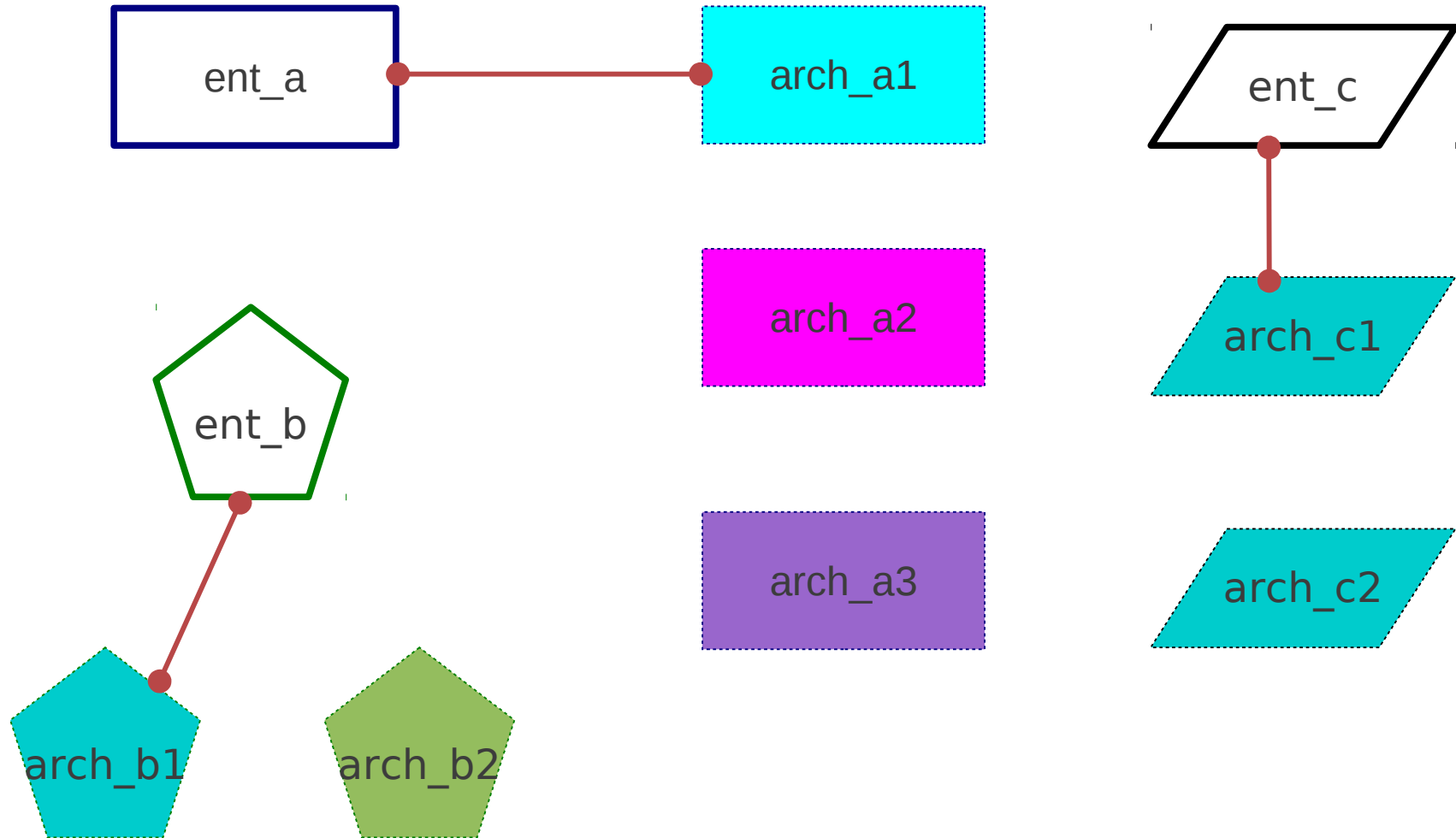


```
architecture arch_a2 of ent_a is  
    port ( ... );  
end ent_a;
```

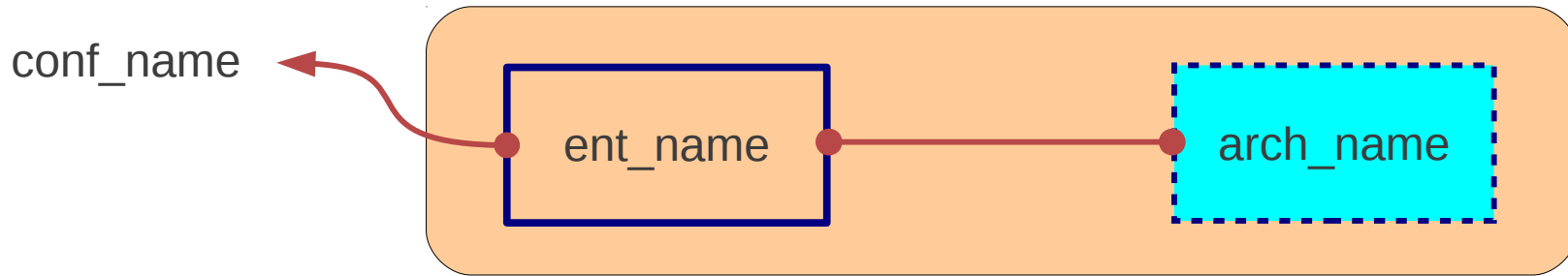


```
architecture arch_a3 of ent_a is  
    port ( ... );  
end ent_a;
```

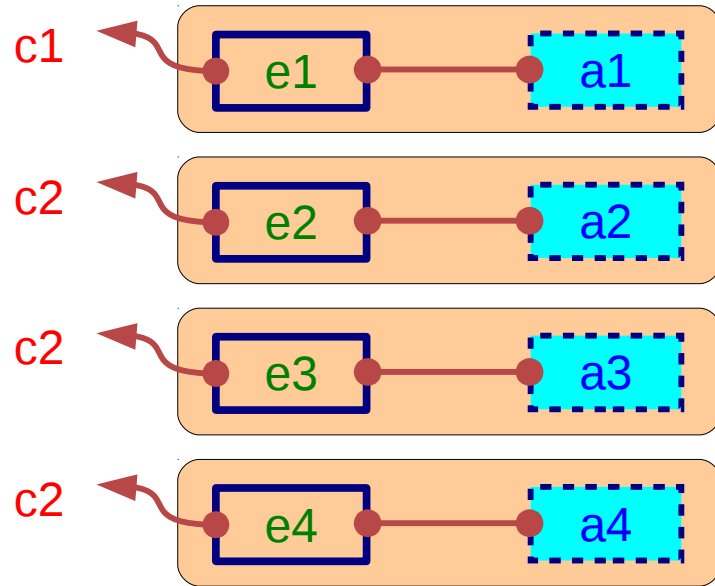
Sequential Assignment (1)



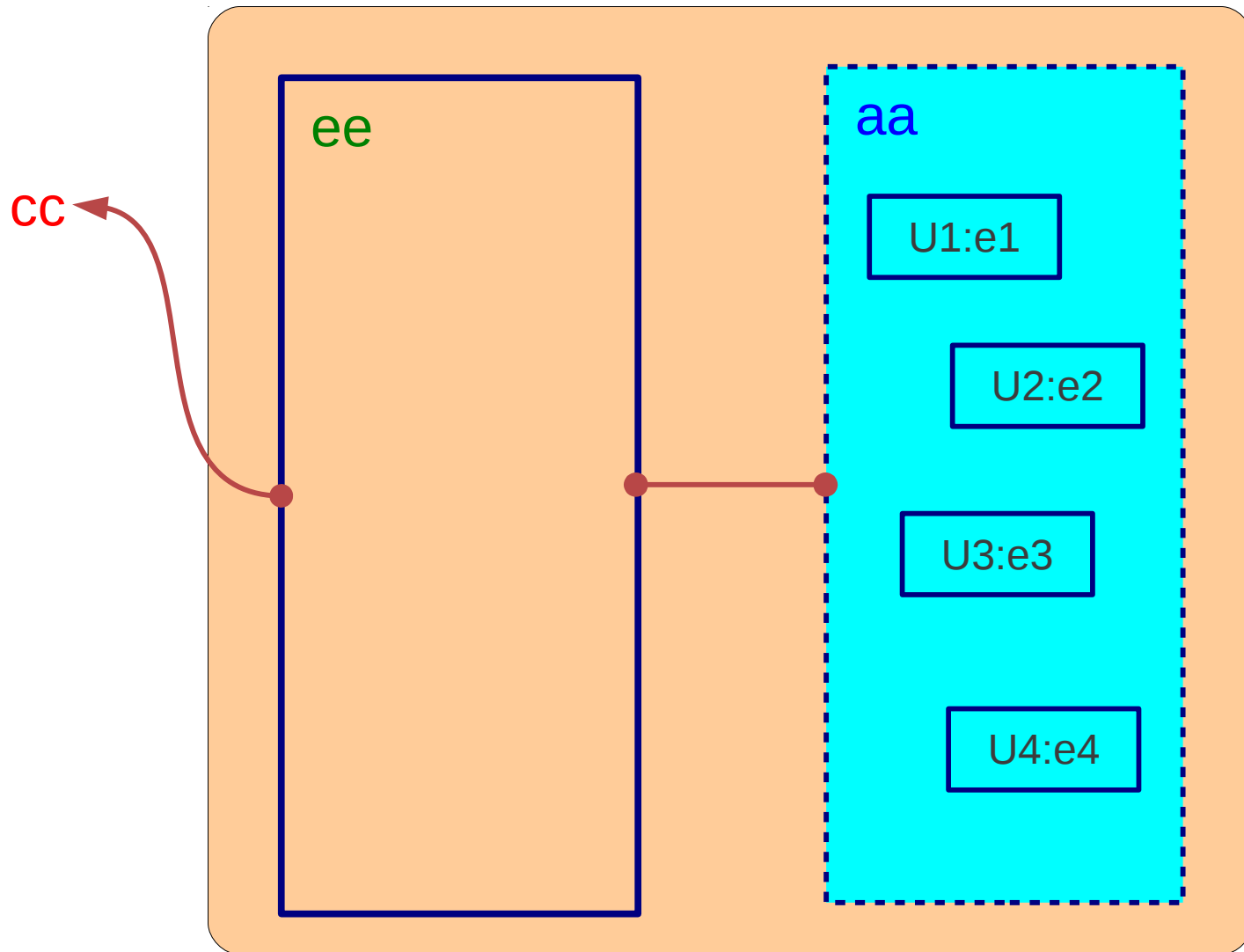
Sequential Assignment (1)



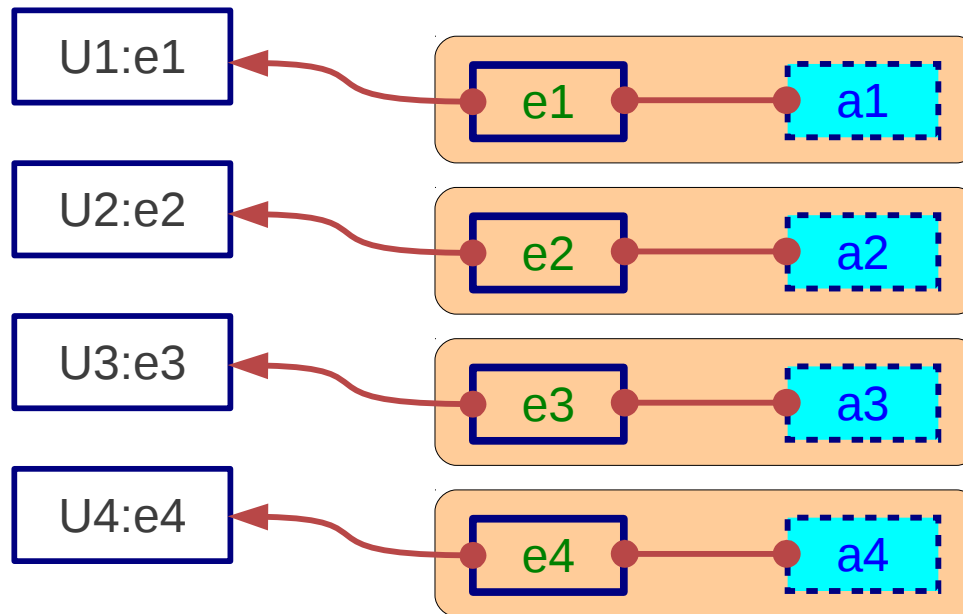
Sequential Assignment (1)



Sequential Assignment (2)



Sequential Assignment (2)



References

- [1] <http://en.wikipedia.org/>
- [2] J. V. Spiegel, VHDL Tutorial,
http://www.seas.upenn.edu/~ese171/vhdl/vhdl_primer.html
- [3] J. R. Armstrong, F. G. Gray, Structured Logic Design with VHDL
- [4] Z. Navabi, VHDL Analysis and Modeling of Digital Systems
- [5] D. Smith, HDL Chip Design
- [6] <http://www.csee.umbc.edu/portal/help/VHDL/stdpkg.html>
- [7] VHDL Tutorial - VHDL online www.vhdl-online.de/tutorial/