Configuration (1A)

Please send corrections (or suggestions) to youngwlim@hotmail.com.

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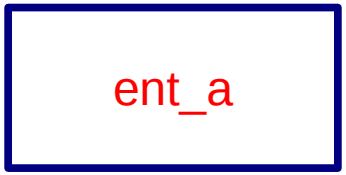
Young Won Lim
04/07/2012

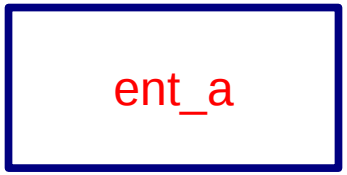
Sequential Assignment (1)



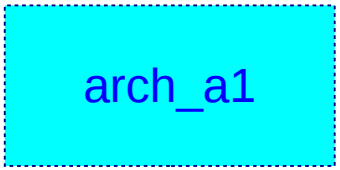

```
entity ent_a is
    port ( ••• );
end ent_a;
```

```
architecture arch_a of ent_a is
    port ( ••• );
end ent_a;
```

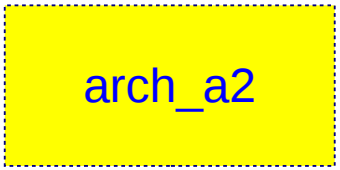
Sequential Assignment (1)



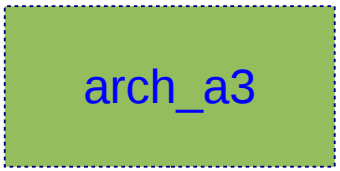

```
entity ent_a is
    port ( ••• );
end ent_a;
```




```
architecture arch_a1 of ent_a is
    port ( ••• );
end ent_a;
```

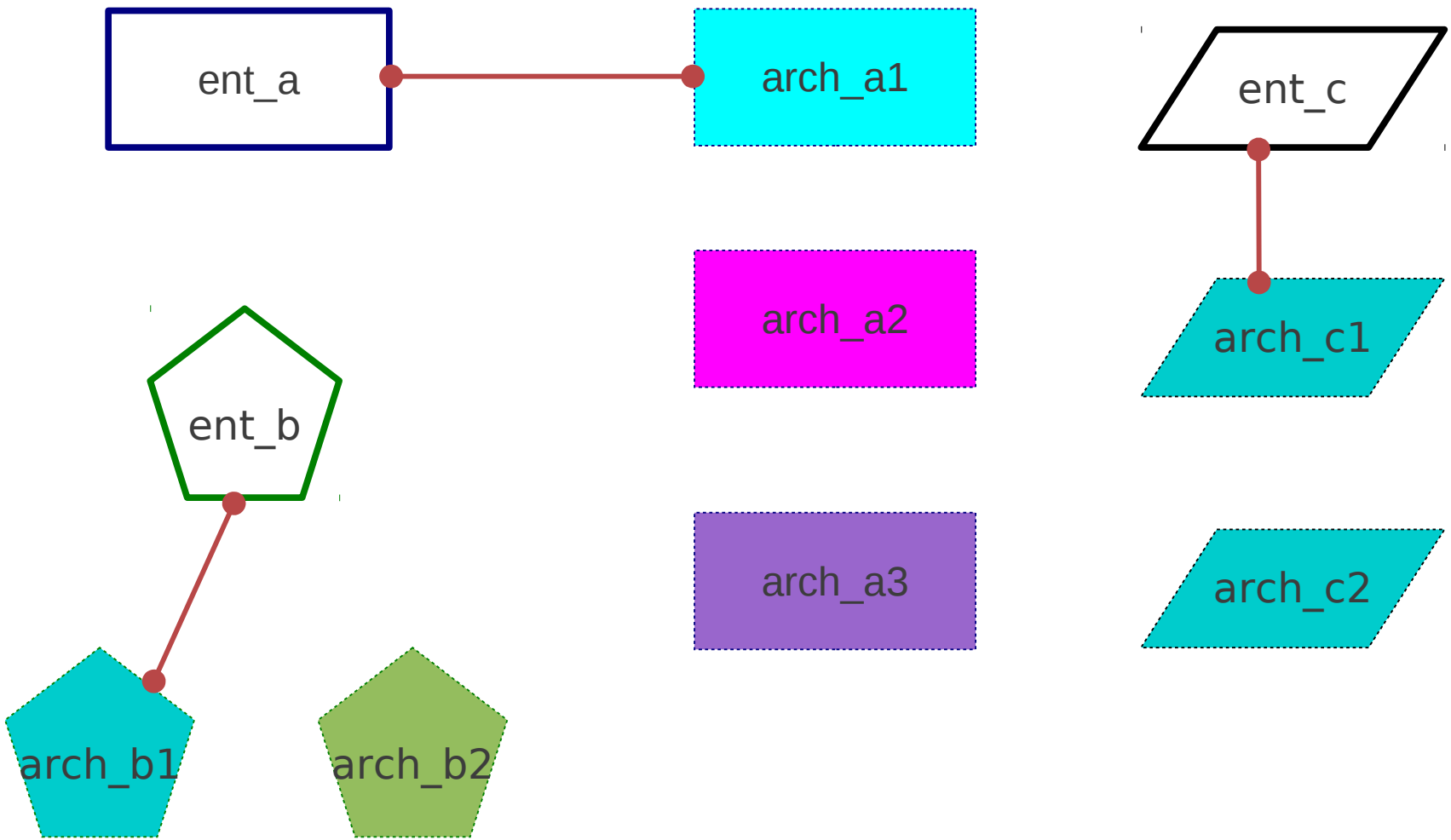



```
architecture arch_a2 of ent_a is
    port ( ••• );
end ent_a;
```

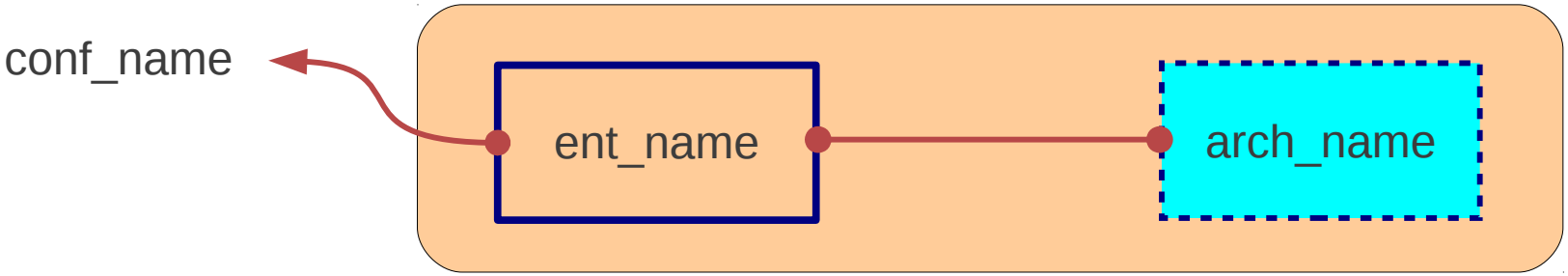



```
architecture arch_a3 of ent_a is
    port ( ••• );
end ent_a;
```

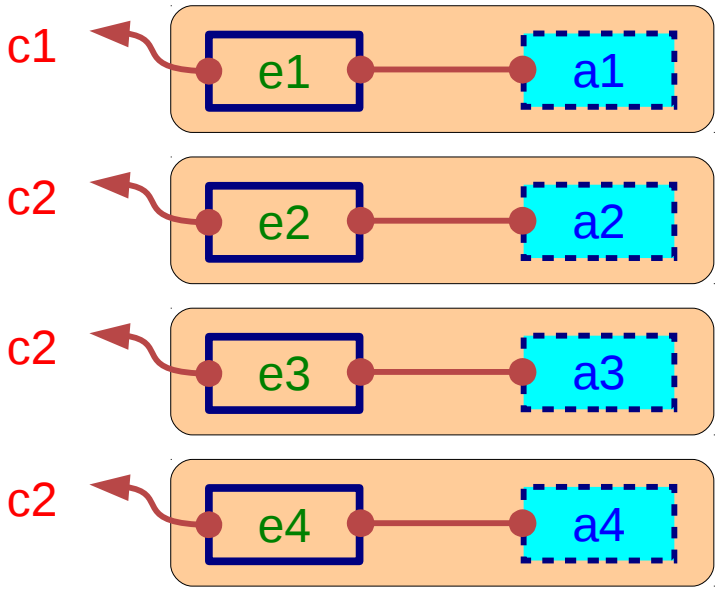
Sequential Assignment (1)



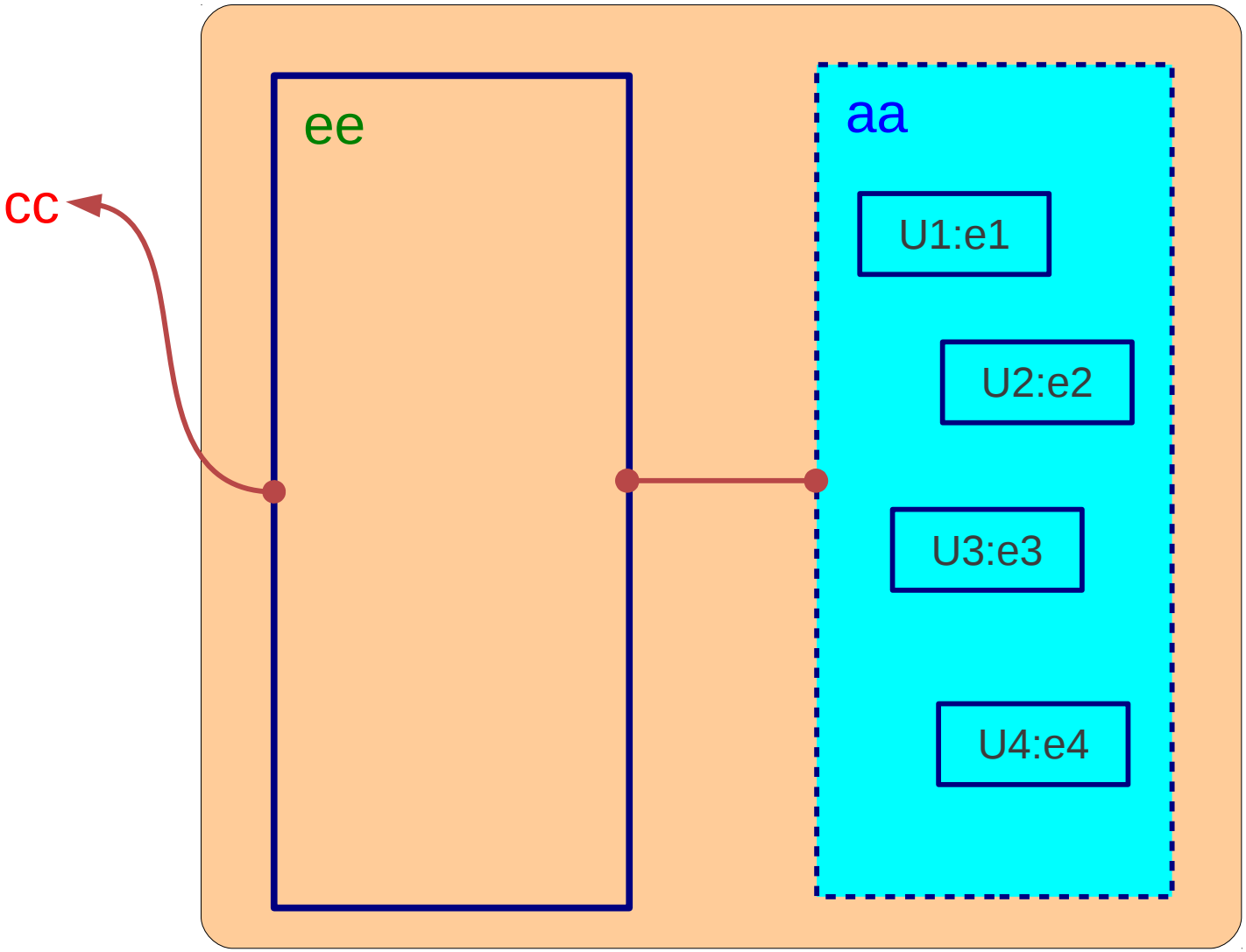
Sequential Assignment (1)



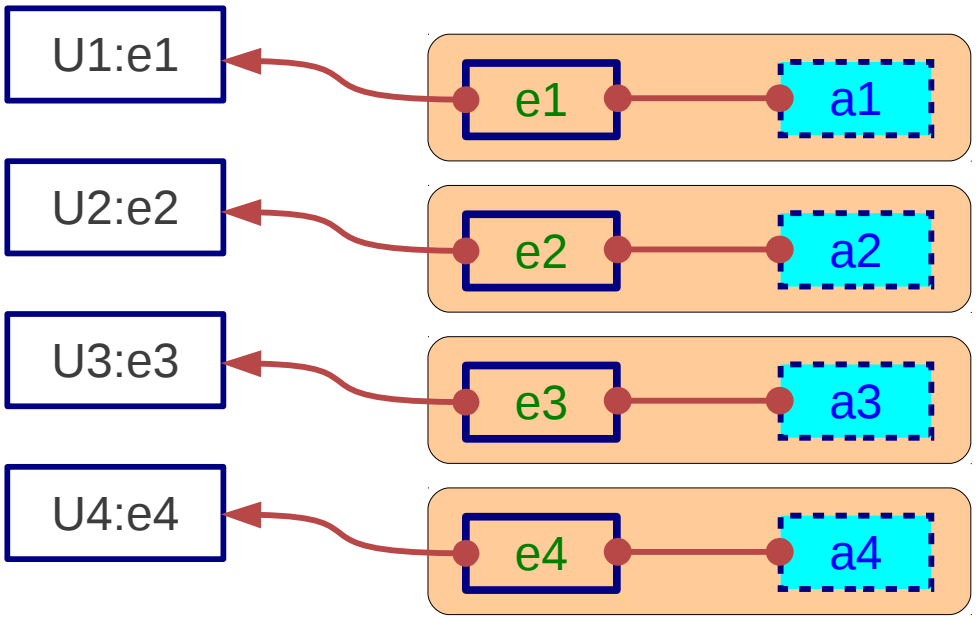
Sequential Assignment (1)



Sequential Assignment (2)



Sequential Assignment (2)



References

[1] http://en.wikipedia.org/
[2] J. V. Spiegel, VHDL Tutorial,
http://www.seas.upenn.edu/~ese171/vhdl/vhdl_primer.html
[3] J. R. Armstrong, F. G. Gray, Structured Logic Design with VHDL
[4] Z. Navabi, VHDL Analysis and Modeling of Digital Systems
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[7] VHDL Tutorial - VHDL onlinewww.vhdl-online.de/tutorial/