2

MOS Amplifier Basics

Overview

This lab will explore the design and operation of basic single-transistor MOS amplifiers at mid-band. We will explore the common-source and common-gate configurations, as well as a CS amplifier with an active load and biasing.

Table of Contents

Pre-lab Preparation

Before Coming to the Lab

Read through the lab experiment to familiarize yourself with the components and assembly sequence. Before coming to the lab, each group should obtain a parts kit from the ECE Shop.

Parts List

The ECE2 lab is stocked with resistors so do not be alarmed if you kits does not include the resistors listed below. Some of these parts may also have been provided in an earlier kit.

Laboratory #2	
MOS Amplifiers	
Qty	**Description**
2	CD4007 CMOS pair/inverter
4	2N7000 NMOS
4	1uF capacitor (electrolytic, 25V, radial)
8	10uF capacitor (electrolytic, 25V, radial)
4	100uF capacitor (electrolytic, 25V, radial)
4	100-Ohm 1/4 Watt resistor
4	220-Ohm 1/4 Watt resistor
1	470-Ohm 1/4 Watt resistor
4	10-KOhm 1/4 Watt resistor
1	33-KOhm 1/4 Watt resistor
2	47-KOhm 1/4 Watt resistor
1	68-KOhm 1/4 Watt resistor
4	100-KOhm 1/4 Watt resistor
1	1-MOhm 1/4 Watt resistor
1	10k trimpot
2	100k trimpot

Background Information

Small-Signal Amplifier Design and Biasing

In earlier experiments with transistors we learned how to establish a desired DC operating condition. If a small time-varying signal is superimposed on the DC bias at the input (gate or base terminal), then under the right circumstances the transistor circuit can act as a linear amplifier. Figure 2-1 illustrates the situation appropriate to a MOSFET common-source amplifier. The transistor is first biased at a certain DC gate bias to establish a desired drain current, shown as the "Q"-point (quiescent point) Figure 2-1a. A small AC signal of amplitude ΔV_{gs} is then superimposed on the gate bias, causing the drain current to fluctuate synchronously. If ΔV_{gs} is small enough, then we can approximate the I_d vs. V_{gs} curve by a straight line with a slope given by

$$g_m = \frac{\partial I_d}{\partial V_{gs}} \tag{2.1}$$

and then the drain current amplitude is $\Delta I_d = g_m \Delta V_{gs}$. With a drain resistor R_d as shown, the drain current is related to the output voltage by $V_{ds} = V_{dd} - I_d R_d$, so the AC output signal will be given by

$$\Delta V_{ds} = -\Delta I_d R_d = -g_m R_d \Delta V_{gs} \tag{2.2}$$

The voltage gain is therefore $A_v = -g_m R_d$. This can be appreciated graphically using a load-line approach as in Figure 2-1b.

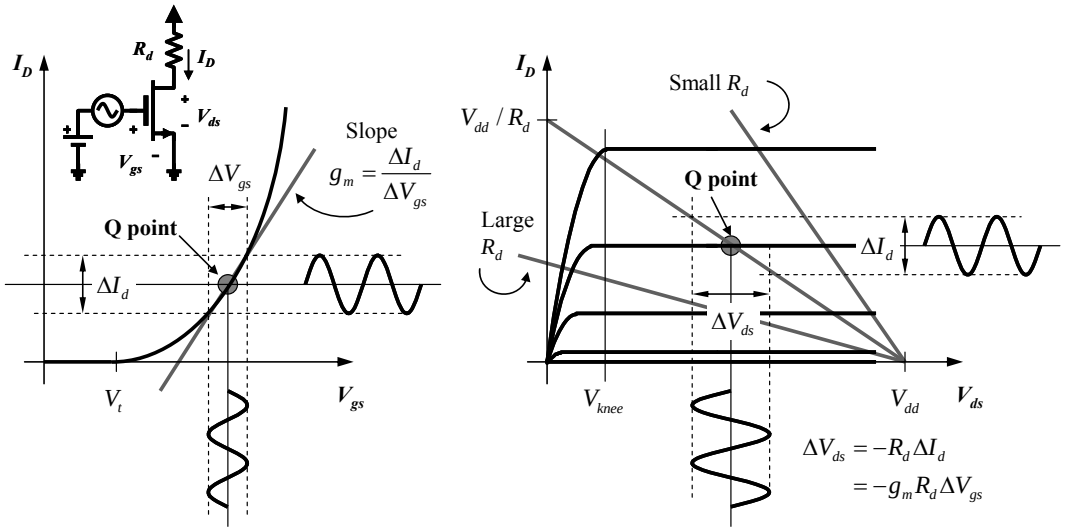


Figure 2-1 – Amplification in a MOSFET common-source configuration. (a) A small AC signal is superimposed on the DC gate bias, creating an AC drain current. (b) Same situation with a load-line superimposed on the output characteristic, showing how the AC drain current leads to an AC drain voltage and gain of $-g_m R_d$.

Figure 2-1 also illustrates the importance of the bias point selection in the operation of transistor amplifiers. Figure 2-1a shows that the transconductance (and hence the gain) will depend on the gate bias; this can be quantified using the I_d vs. V_{gs} characteristic

$$I_m = K_n \left(V_{gs} - V_t\right)^2 \tag{2.3}$$

Substituting (2.3) into (2.1) gives

$$g_m = 2K_n(V_{gs} - V_t) = 2\sqrt{K_n I_d} = \frac{2I_d}{(V_{gs} - V_t)} \tag{2.4}$$

To establish a large transconductance we must bias the device well above threshold. This is also important to insure that the transistor stays in saturation over the full AC cycle. However, there is a limit on gate bias and drain current imposed by the output characteristic and load resistor as shown in Figure 2-1b. To allow for maximum output voltage swing the Q-point should lie approximately halfway between V_{dd} and the edge of the ohmic region, shown in the figure as V_{knee}. If the drain current or load resistor is too large, the device will swing into the ohmic region during operation leading to significant waveform distortion.

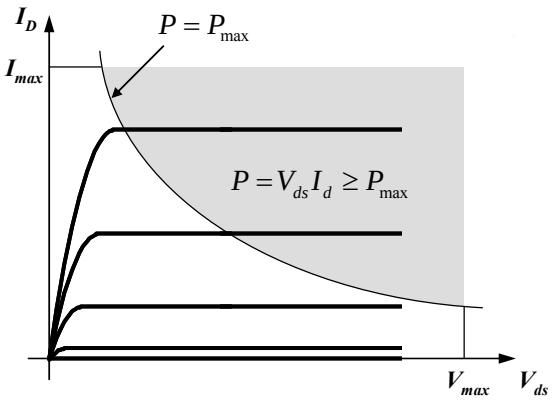


Figure 2-2 – Limitations on biasing imposed by maximum power considerations.

Another important consideration is the DC power dissipation in the device given by $P = V_{ds} I_d$. This power is dissipated as heat within the device so there is always a thermal limit on the dissipated power for every device and package. The datasheet will specify the maximum DC power $P_{\max}$, maximum DC current $I_{d\max}$, and maximum DC voltage $V_{ds\max}$, to avoid destroying the device. These limits are superimposed on the output characteristic in Figure 2-2. The Q-point must be selected to lie below the shaded region in the figure.

Although the focus has been on MOSFETs in this discussion, it is important to recognize that the key conclusions above are largely independent of the choice of device. All transistors can be described by an output-current versus input-voltage characteristic like that in Figure 2-1a, and hence by a bias-dependent transconductance. Only the details of the voltage dependence will be different. For example, BJTs follow a diode-like exponential model; state-of-the-art short-channel MOSFETs have a nearly linear I_d vs. V_{gs} characteristic and hence a constant g_m.

Lastly, note that the supply voltage is also an important variable. Generally a larger supply voltage is desirable for maximum voltage gain and maximum output voltage swing. This can be seen as follows: for a given drain current I_d, the drain resistor that is required for a drain bias of $V_{ds} \approx V_{dd}/2$ is

$$R_d = \frac{V_{dd} - V_{ds}}{I_d} \approx \frac{V_{dd}}{2I_d} \tag{2.5}$$

and thus the gain is given by

$$\left|A_v\right| = g_m R_d \approx \frac{g_m}{I_d}\frac{V_{dd}}{2} = V_{dd}\sqrt{\frac{K_n}{I_d}} \tag{2.6}$$

The maximum gain scales with supply voltage for a specified device and current level.

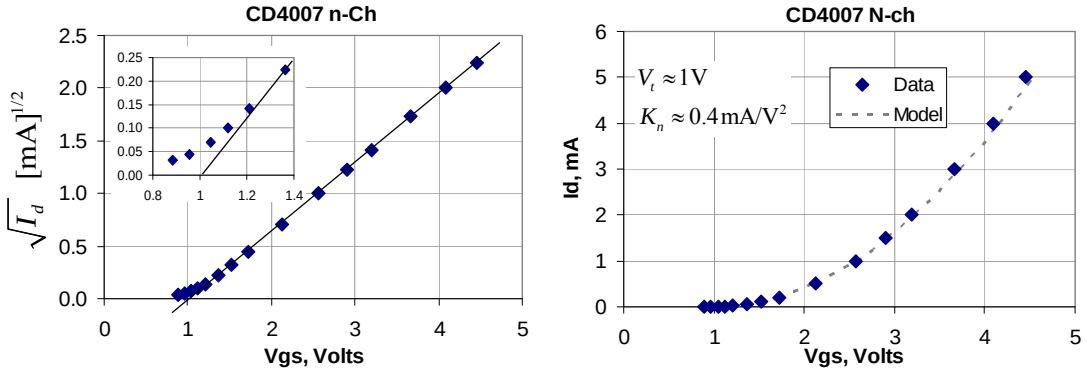
MOSFET Design Parameters and Subthreshold Currents

For amplifier designs using any transistor (MOSFETs or BJTs) we need to know the transconductance g_m. For MOSFETs, a knowledge of the threshold voltage V_t and the current parameter K_n can be used to estimate g_m using (2.4), ***assuming the square-law device model (2.3) holds***. A common method to estimate these parameters is to measure and plot the square-root of I_d versus V_{gs}, which theoretically should yield a linear dependence,

$$\sqrt{I_d} = \sqrt{K_n}\left(V_{gs} - V_t\right) \tag{2.7}$$

Thus the x-intercept if such a plot should yield the threshold voltage, and the slope should yield the current parameter.

This method works reasonably well for older MOSFET technologies with gate lengths of >2μm; such devices are reasonably well modeled by a square-law characteristic in saturation. For example, Figure 2-3a shows such a plot for the 6-7-8 NMOS device in the CD4007 chip; these devices have gate lengths of ~10μm. Clearly the data is well modeled by the linear dependence predicted in (2.7) for most of the anticipated gate-bias range. For this particular data set we find $V_t \approx 1\text{V}$ and $K_n \approx 0.4\,\text{mA/V}^2$ (remember that threshold voltages can vary significantly from one device to another, so don't assume these values hold for your amplifiers!).



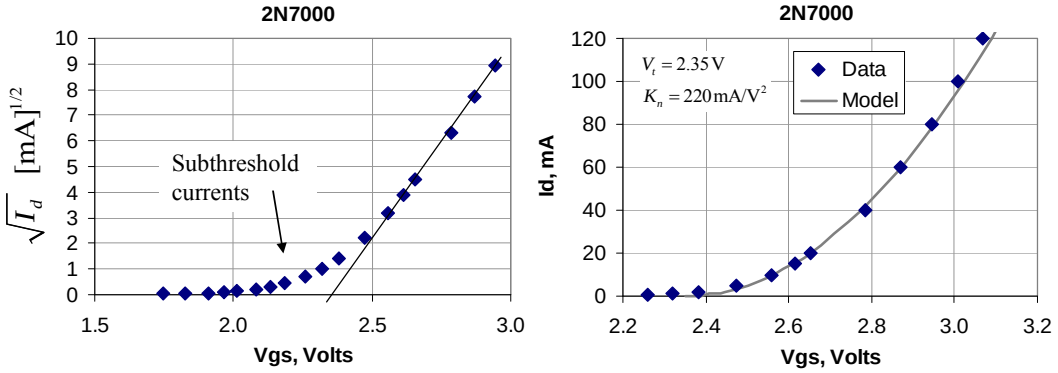
(a) (b)

Figure 2-3 – (a) Measured data for one NMOS device in the CD4007 chip, plotted as $\sqrt{I_d}$ vs. V_{gs}, showing the linear dependence characteristic of a long-channel square-law device. (b) Same data set plotted as I_d vs. V_{gs}, with comparison to the ideal model using given parameters (dashed line).

Near the threshold voltage in Figure 2-3a you can start to see some small departure from the square-law characteristic, which is typical of all MOS devices. Ideally the current should go to zero at the threshold voltage, but in real devices it just tails off exponentially and never quite goes to zero. This is called "subthreshold conduction", and the details are beyond the scope of our discussion here. The effect is significant only if we intend to operate the device near threshold. For linear amplifiers using the CD4007, that is unlikely. Why? The MOSFETs in the CD4007 are small, with gate widths of 30μm, and have a low $\mu_n C_{ox}$ product. Consequently they can not carry much current (the data sheet says 10mA is the absolute maximum) and the transconductance is rather small. To get a nice voltage gain from these devices we will need to maximize the $g_m R_d$ product, and for this particular device that means we need to operate well above threshold. Even at a drain bias of ~5mA, which is about as high as we can safely go, the transconductance is only ~3mS. So, as far as the

CD4007 is concerned, we will always be operating it well above threshold where the device is very well modeled by a square-law characteristic.

The 2N7000, also in your parts kit, is at the other extreme: it is intended for larger currents and has an inherently larger transconductance. Consequently we need to operate this device closer to threshold in order to keep the DC currents low, an imperative from a DC power-dissipation standpoint. The data sheet specifies a maximum DC power dissipation of 400mW; for drain voltages in the range of 2.5-5V (appropriate to supply voltages in the range of 5-10V) we would need to keep the currents below ~100mA. Figure 2-4 shows a measured plot of $\sqrt{I_d}$ vs. V_{gs} for a 2N7000 for currents in this range; on this scale we can see a significant departure from the square-law characteristic. This device has gate lengths of around 2.5um.



(a) (b)

Figure 2-4 – (a) Data for a 2N7000 device plotted as $\sqrt{I_d}$ vs. V_{gs}, showing sub-threshold currents. (b) Same data set plotted as I_d vs. V_{gs}, with comparison to the ideal model using given parameters (dashed line)

Is this a problem? No, it just means that we can't expect (2.3) to work well below currents of around 10mA. Above 10mA, the model seems to work reasonably well, and for the particular device shown in Figure 2-4 we find $V_t \approx 2.35\,\text{V}$ and $K_n \approx 220\,\text{mA/V}^2$.

Remember, these parameters vary from device to device, and also may vary considerably from manufacturer to manufacturer. Figure 2-5 shows a comparison of characteristic from four different 2N7000 devices, two from one manufacturer, and two from another manufacturer, selected randomly. Not only does the threshold voltage vary, but it is apparent that the current parameter K_n also varies between manufacturers.

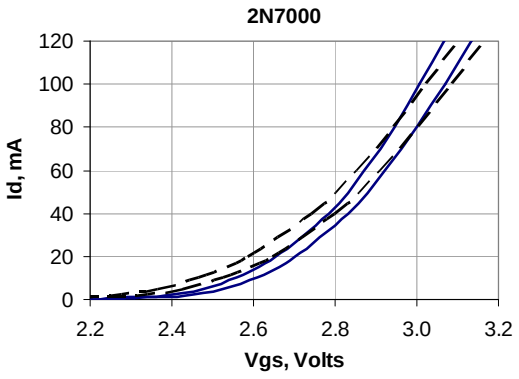


Figure 2-5 – Comparison of four different 2N7000 devices. Dashed lines and solid lines represent different manufacturers.

Frankly the 2N7000 isn't a great choice for small-signal linear amplifier designs, it is really intended for use in power switching circuits. You might wonder why we chose the 2N7000 for this experiment. The simple answer: it is cheap and ubiquitous, a common theme for components used in ECE 2 labs!

Estimating Key Device Parameters

Measurements like those in Figure 2-3 and Figure 2-4 are great if you have them, but they take some time to generate. For simple amplifier design we just need a rough estimate of the device parameters, and the circuit in Figure 2-6 can be used for a quick estimate of g_m and V_t.

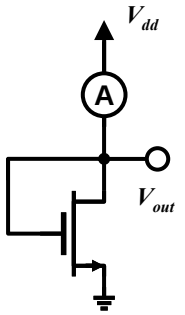


Figure 2-6 –Circuit for estimating FET parameters.

Recall that connecting the drain and gate terminals forces the FET to operate in saturation for any bias above threshold, so simply varying the supply voltage V_{dd} allows us to map out any part of the I_d vs. V_{gs} characteristic in saturation. The procedure for determining g_m is then as follows: adjust the supply voltage so that the ammeter reads the desired bias current I_d, and record the gate voltage. Next, change the supply voltage just a little, so that the gate voltage changes by a small amount (e.g. $\Delta V_{gs} = 50\,\text{mV}$), and record the resulting small change in drain current ΔI_d. The transconductance is then approximated by

$$g_m \approx \frac{\Delta I_d}{\Delta V_{gs}} \tag{2.8}$$

A similar procedure can be used to find the threshold voltage, but for this step we must assume that our square-law model holds. Start again with a supply voltage that gives the desired drain current I_d; if we define V_{gs1} as the corresponding gate voltage, then

$$I_d = K_n \left(V_{gs1} - V_t\right)^2 \tag{2.9}$$

Now, increase the supply voltage so that the drain current increases by a factor of four. This happens at a new gate voltage V_{gs1}, such that

$$4I_d = K_n \left(V_{gs2} - V_t\right)^2 \tag{2.10}$$

Equations (2.9) and (2.10) can now be solved for the threshold voltage, giving

$$V_t \simeq 2V_{gs1} - V_{gs2} \tag{2.11}$$

Once the threshold voltage is known, K_n can be determined by substituting back into (2.9).

It must be remembered that the step outlined above for determining the threshold voltage depends on the use of a square-law model for I_d vs. V_{gs}. We have already seen that this model does not work well near threshold. Many modern FETs with short channel also follow a different model. *So this method only works well for older, long-channel devices and at suitably chosen currents.*

In summary, using the circuit in Figure 2-6 allows the device parameters to be estimated quickly as follows:

1. Adjust the supply voltage V_{dd} to establish a desired drain current I_d, and record the corresponding gate voltage V_{gs1}
2. Increase V_{dd} slightly so that V_{gs} increases by a small fixed amount (e.g. 50mV), then find g_m using (2.8)
3. Increase the supply voltage further until the drain current increases to $4I_d$, record the corresponding gate voltage V_{gs2}, and find the threshold voltage from (2.11)
4. Use one of the data points above and your estimate of V_t to determine K_n

In-Lab Procedure

2.1 Common-Source Amplifier

Common-Source, no Source Resistor

Figure 2-7 shows the basic common-source amplifier with no source resistance. We have learned that this topology is intolerant of device variations, specifically gate threshold variations, but it is nevertheless a good place to start our experimentation. The only new additions to the circuit in comparison to the biasing networks we built in ECE 2B are the AC coupling capacitors. In this lab we will use rather large capacitors and focus just on the mid-band gain; the next lab will explore the impact of these capacitors on the frequency response.

- □ Using the technique described in the background section, find the transconductance for your 2N7000 devices assuming a desired bias current of $I_d \approx 20\,\text{mA}$, and also find the threshold voltage and current parameters.
- □ Using the circuit of Figure 2-7 and the parameters you found in the previous section, choose a suitable resistor R_{g1} that will give a DC drain bias current of $I_d \approx 20\,\text{mA}$ (within 20% of that goal is fine) such that $V_d \approx V_{dd}/2$. Feel free to use a trimpot or a decade box for R_{g1}. Record the resistance value and resulting DC drain current and drain voltage.
- □ Next, apply a 0.1V amplitude 1kHz sine-wave at the input terminal using your bench function generator, and record the input and output waveforms on the oscilloscope. Be sure to use the correct polarity for the coupling capacitors.

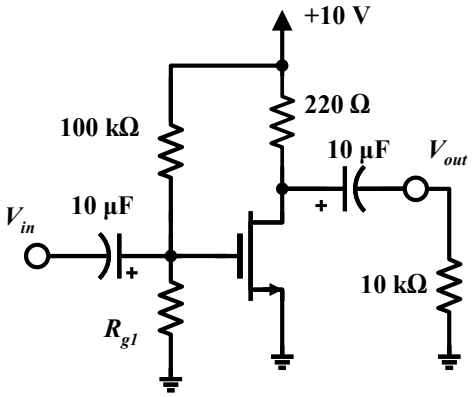


Figure 2-7 – Common-source amplifier

- □ What is that voltage gain for this circuit? Compare with the simple result $A_v = -g_m R_d$ for the common-source amplifier.
- □ Replace the 220Ω drain resistor with a 100Ω resistor and re-measure the voltage gain (the drain current should not change much since this is determined by V_{gs}). Compare again to the theoretical gain.

Linearity and Waveform Distortion

Note that we have thus far kept the input signal very small, well within the "small-signal" requirement. As the input signal is increased in amplitude, eventually the small-signal model breaks down and the nonlinearity of the device becomes important. This is manifest as significant waveform distortion in the output signal.

- □ Using the circuit of Figure 2-7 with the 220Ω drain resistor, double the amplitude of the input signal to a 0.2V amplitude sinusoid at 1kHz. Can you begin to see asymmetry in the output signal? Record your observations.
- □ Increase the input signal to 0.5V and record the result.

The output signal can become distorted even for small input signals if the gain is too large or the bias point is poorly chosen. In that case the output signal swing may be large enough to causes the device to enter the Ohmic region of operation during part of the cycle.

□ Return the function generator to a 0.1V amplitude sinusoid, but swap the 220Ω drain resistor for a 470Ω resistor. Now record the output waveform. Can you explain why there is signal distortion in this case?

Effect of Source and Load Impedances

In the above experiments we have tested the amplifier under somewhat ideal conditions: using a source (the function generator) with a small source resistance, and a high-impedance load (the 10k resistor). In practice the source and load impedance may be comparable to the circuit impedances and can have a measurable effect on the amplifier performance. Figure 2-8 shows a modified circuit with these additional resistances. Note that V_{sig} and R_{sig} simply represent the Thevenin equivalent for *any* circuit that drives the amplifier under test. In a real application this might be another transistor amplifier stage. For lab experiments we usually use a function generator, in which case the source resistance is shown on the front panel.

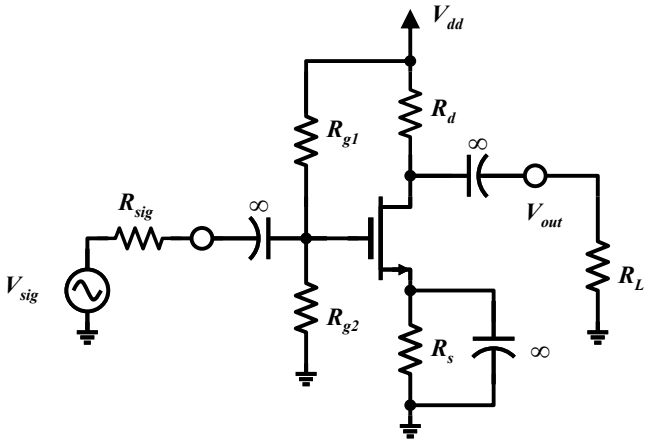


Figure 2-8 – CS amp with source and load impedances.

□ Starting again with the circuit of Figure 2-7, add a load resistance $R_L = R_d$ at the output terminal and re-measure the voltage gain under small-signal conditions. Is your result consistent with the theoretical output impedance of the CS amplifier ($R_{out} \approx R_d$)? If not, why?

□ Similarly, add a series resistance R_{sig} that is approximately equal to the input resistance you would expect for your amplifier (in this case, $R_{g1} \,||\, R_{g2}$), and record the voltage gain.

□ From your measurements, tabulate the following results for your amplifier: input impedance, output impedance, and open-circuit voltage gain.

□ Find and record the source resistance of the benchtop function generator, and the input resistance of the oscilloscope. From this information and the results of your measurements above, describe (in your lab report) whether the function generator and oscilloscope had any significant effect on the measurement of your amplifier.

Common-Source with Source Resistor

You may recall that the addition of a source resistance is advantageous in order to stabilize the circuit with respect to threshold voltage variations. However, this has a detrimental effect on the gain, which we can see as follows:

- □ Construct the circuit of Figure 2-9. You will need to change the gate bias network (R_{g1}) in order to keep the drain current constant at around 10mA (something like 100k should work well for most devices).
- □ Now measure the voltage gain under open-circuit load conditions and with a 0.1V input sinusoid at 1kHz. Why has the gain changed?

There is a simple trick to overcome this limitation: simply add an AC bypass capacitor around the source resistance!

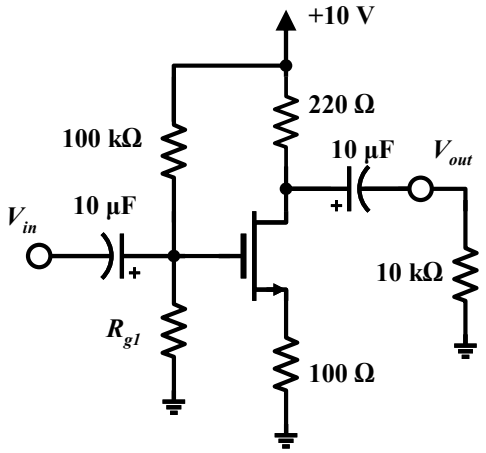


Figure 2-9 – Adding a source resistance.

- □ Add a 10µF capacitor in parallel with the source resistance and re-measure the voltage gain. Compare with the original circuit without the source resistance.
- □ Explore the performance of the circuit with respect to device variations by swapping in a different 2N7000 device and re-measuring the DC drain current, DC drain voltage, and AC voltage gain.
- □ Include a complete AC/DC analysis of this circuit in your lab report with comparison to your measured results.

2.2 Common-Gate Amplifier

With a small modification to the previous circuit we can implement a common-gate amplifier, as shown in Figure 2-10. Note the 100µF AC coupling capacitor at the input, and the 10µF bypass capacitor on the gate; the latter makes the gate an AC ground, appropriate to the common-gate configuration.

- □ Construct the circuit in circuit Figure 2-10. Be sure to use the correct polarity for the coupling capacitors, or the circuit may not function properly.
- □ With the power supply on, the function generator connected to the input port, and the oscilloscope set to observe the input voltage V_{in}, adjust the amplitude of the function generator such that V_{in} is a 50mV sinusoid at 1kHz. Then measure and record the AC voltage gain V_{out}/V_{in} and compare with theory.
- □ You can appreciate the importance of source resistance and input resistance considerations in this circuit with the following test: with the amplifier configured as in the previous step

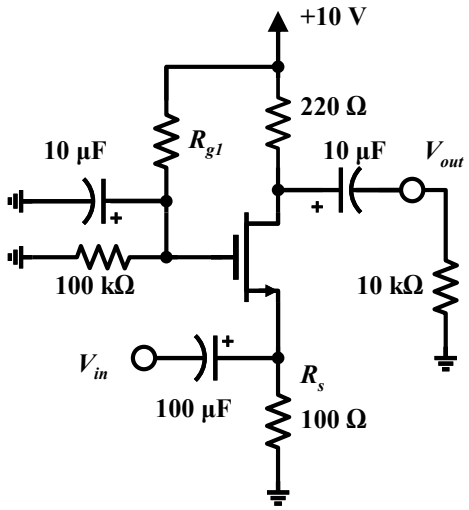


Figure 2-10 – Common-gate amplifier.

and the oscilloscope set to observe V_{in}, *turn off* the +10V power supply to the circuit. The input waveform should change significantly. Why?

In addition to the non-inverting nature of this amplifier, the key difference in comparison to the CS amplifier is the input resistance, which is approximately $R_{in} \approx 1/g_m$. We will talk more about this in lecture and in connection with the frequency response in later labs. In this case, the low input resistance forms a voltage divider with the function generator. When the transistor is unbiased (off), R_{in} the input resistance is approximately $R_{in} = R_s = 100\Omega$, and when it is biased on, the input resistance is the parallel combination of R_s and $1/g_m$.

□ Using the source resistance of the function generator, calculate the actual signal voltage V_{sig} from your measurement of V_{in} in the unbiased state, and use this to determine the overall gain of the circuit, V_{out}/V_{sig}.

The low input resistance also means that we must use a larger AC coupling capacitor at the input, to keep the RF time constant large enough for operation at 1 kHz. You can see the importance of this consideration in the following test:

□ Replace the 100μF input capacitor by a 1uF capacitor and re-measure the voltage gain. Record and explain your observations.

2.3 Amplifiers with Active Loading

Feedback-Bias Amplifier

You may recall seeing the feedback-bias arrangement shown in Figure 2-11a from lecture and homework assignments last quarter. This is attractive because it forces the device to stay in saturation. Otherwise, the circuit is similar in most respects to the common-source amplifier we constructed earlier: the voltage gain is approximately $A_v = -g_m R_d$.

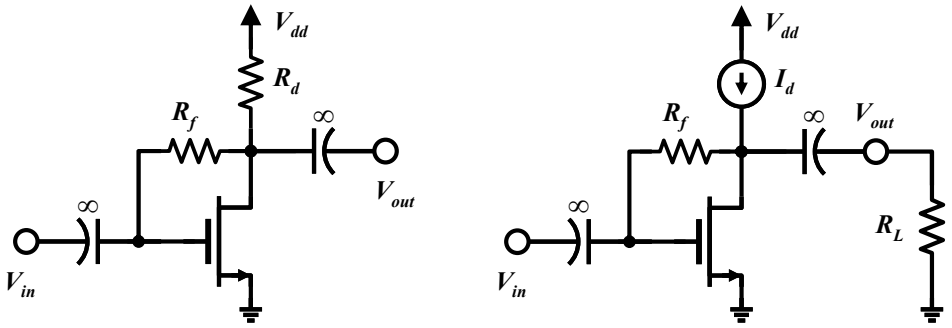


Figure 2-11 – (a) Feedback-bias amplifier configuration, and (b) Similar circuit with drain bias set with current source instead of a resistor.

A drawback with this and our earlier CS amplifier is that the drain resistor R_d simultaneously controls the gain and the drain bias point. As we saw earlier, if the drain resistance is increased in an attempt to increase the gain, the drain bias point is reduced and

hence the allowable signal swing at the output is reduced. In contrast, the circuit of Figure 2-11b uses a constant-current bias to set the drain current. Since the effective impedance of a current-source is infinite, the voltage gain in this case will be set by the load resistance, ie. $A_v \approx -g_m R_L$. In other words, using a constant-current-source biasing, we can decouple the gain and bias so that each can be adjusted independently.

Constant-current biasing can be accomplished with circuits like the one shown in Figure 2-12. Here Q3-Q4 are used to set a constant gate bias for Q2, which serves as constant-current source for Q1; this is called *active loading*. However, Q2 is not an ideal current source; it has a finite output resistance given by $r_o = |V_A|/I_d$, where $|V_A|$ is the Early voltage. So in this case the gain will become $A_v \approx -g_m (r_o \| R_L)$. The open-circuit gain $g_m r_o$ is sometime called the *intrinsic* gain of the circuit.

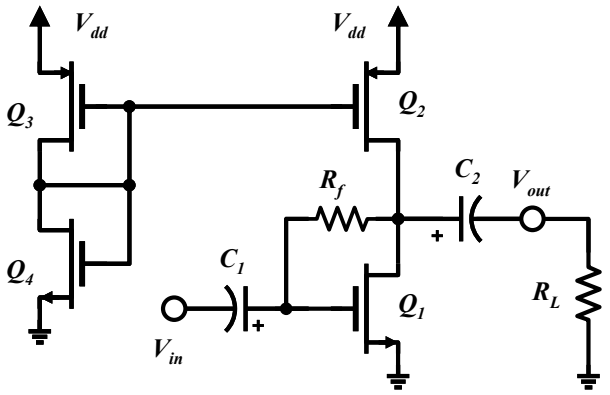


Figure 2-12 – CMOS common-source amplifier with active (constant-source) biasing.

You may wonder why we didn't just use a resistor divider to set the bias point for Q2 instead of Q3-Q4. We certainly *could* make a working circuit that way, but in integrated circuit design it is more size- and cost-efficient to use transistors than resistors whenever possible. Secondly, active bias networks can also be designed so that the bias-point to automatically adjusts for device variations induced by temperature changes. That is a topic you will take up in ECE 137AB.

CMOS Active-Load CS Amplifier

Let's build the circuit Figure 2-12 using the CD4007. For convenience we have included the CD4007 pinout and equivalent circuits in Figure 2-13 below.

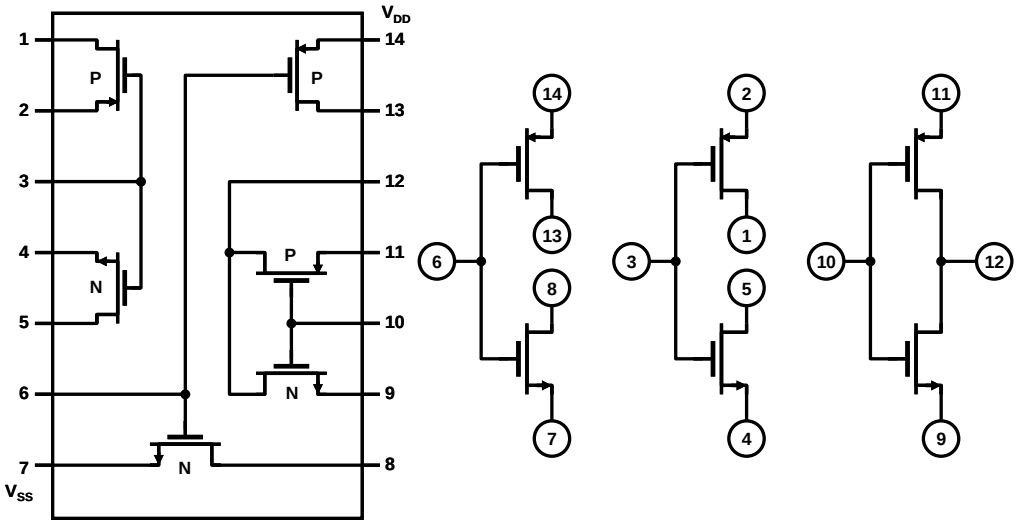


Figure 2-13 – CD4007 pinout and simplified schematics.

NOTE: remember that pins 14 and 7 must ALWAYS be connected to Vdd (the positive supply) and Vss (the negative supply, or ground in this case) no matter which devices are being used:

- □ As a first step, measure the transconductance g_m assuming a drain current of ~5mA, and also measure the threshold voltage V_t and current parameter K_n using the method we discussed earlier in the background section (currents from 2mA to 8mA are a good choice). Measure one each of the n-channel and p-channel devices.
- □ Next, with the help of Figure 2-13, add pin numbers to the schematic of Figure 2-12 to make assembly easier. Because of the common gate connections in the paired devices, so you will need to use devices from separate pairs for Q1 and Q2.
- □ Now, assemble the circuit of Figure 2-12 using $V_{dd} = +10\,\text{V}$, $R_f = 1\text{M}\Omega$, and 1μF coupling capacitors (C_1 and C_2). Be sure to use the correct polarity of the coupling capacitors, or the circuit may not function properly.
- □ Measure the DC voltages at the gate of Q2 and the drain of Q1. From this, estimate the current in Q1 and the transconductance at this current using your model parameters.
- □ Apply a 0.1V sinusoid at 1 kHz to the input and record the input and output waveforms under open-circuit load conditions. Record this intrinsic voltage gain.
- □ Now add a load resistor $R_L = 10\,\text{k}\Omega$ and re-measure the gain. From the reduction in gain, estimate the output resistance $R_{out} = r_o$ of the amplifier, and compare the measured intrinsic gain with the theoretical $g_m r_o$.
- □ Now add a load of $R_L = 1\,\text{k}\Omega$ and measure the gain. How does it compare with the theoretical $A_v \approx -g_m \left(r_o \,||\, R_L \right)$?

Congratulations!
You have now completed Lab 2

